

# Jedi 15"/17" Schematics

## Comet Lake - U/2GB VRAM

2019-06-06

REV : A00

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*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DISCRTE OPTIMUS installed*

Jedi15"/17" CML



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**Jedi15"/17" CML**

Rev

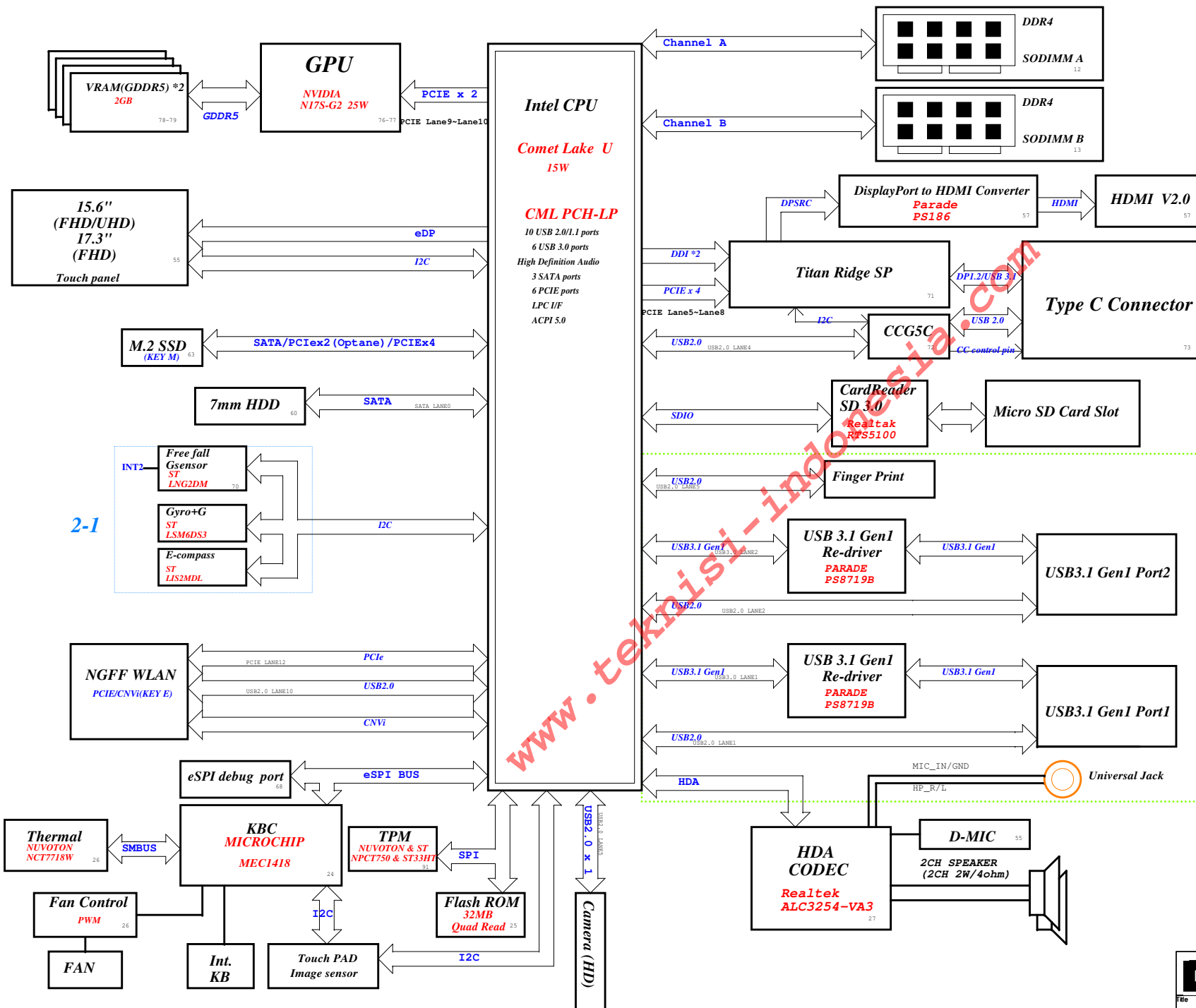
**A00**

Date: Monday, June 10, 2019

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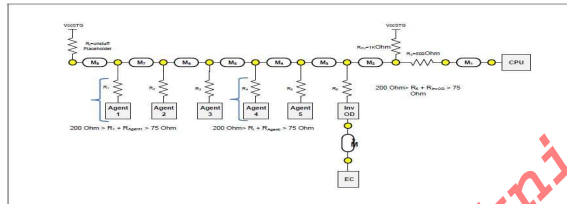
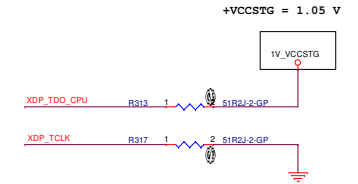
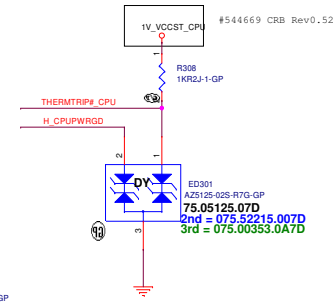
# Jedi 15"/17" CPU 15W + GPU 25W Block Diagram

Project code: 4PD0HC010001  
PCB P/N: 18806  
Revision: A00



IO Board

24	PECI_CPU		
24,44,46,72	PROCHOT#_CPU		
55	TOUCH_PANEL_INTR#		
24,65	TP_WAKE_KBC#		
55	TOUCH_PANEL_PD#		
17	H_CPUPWRGD		



Reference	Via Count	Max Length, mm		Max Length, Mils	
		Segment	Total	Segment	Total
SS	2	38		1496.06	
SS	2	279		10984.3	
SS	1	76		2992.13	

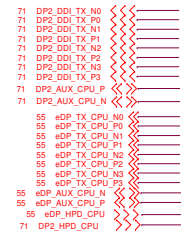
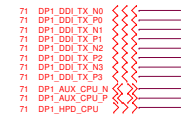
## Topology Guidelines

Platform resistors values	$R_{pu}=1K\Omega$ , $R_s=500\Omega$ , $R_i+R_{agent}=75-200\Omega$ , $R_6+R_{invod}=75-200\Omega$
---------------------------	---

Platform resistors tolerances	$\pm 5\%$
-------------------------------	-----------

Main Func = CPU

DP to TR



eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 $\Omega$ $\pm 1\%$	Max = 600 mils

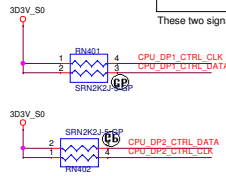
DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

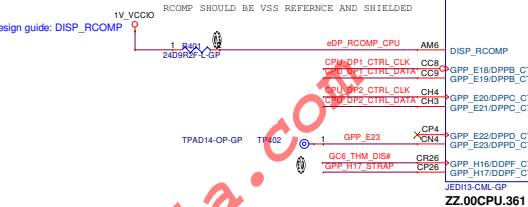


Port 1

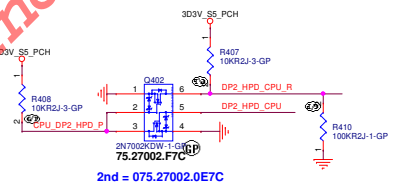
DP to TBT

Port 2

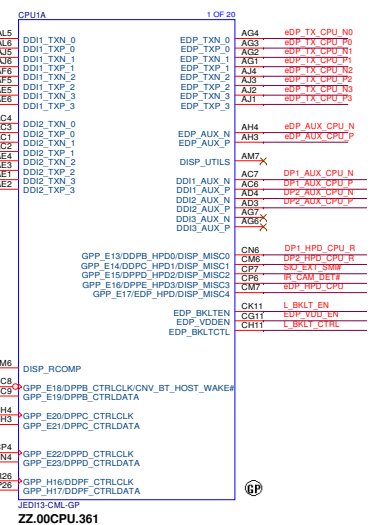
CHECK WHL design guide: DISP\_RCOMP



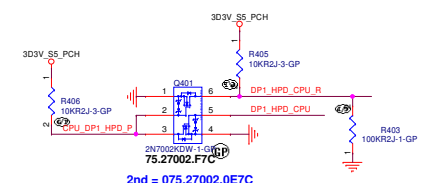
SD EXT SM



2nd = 075.27002.0E7C



ZZ.00CPU.361



2nd = 075.27002.0E7C

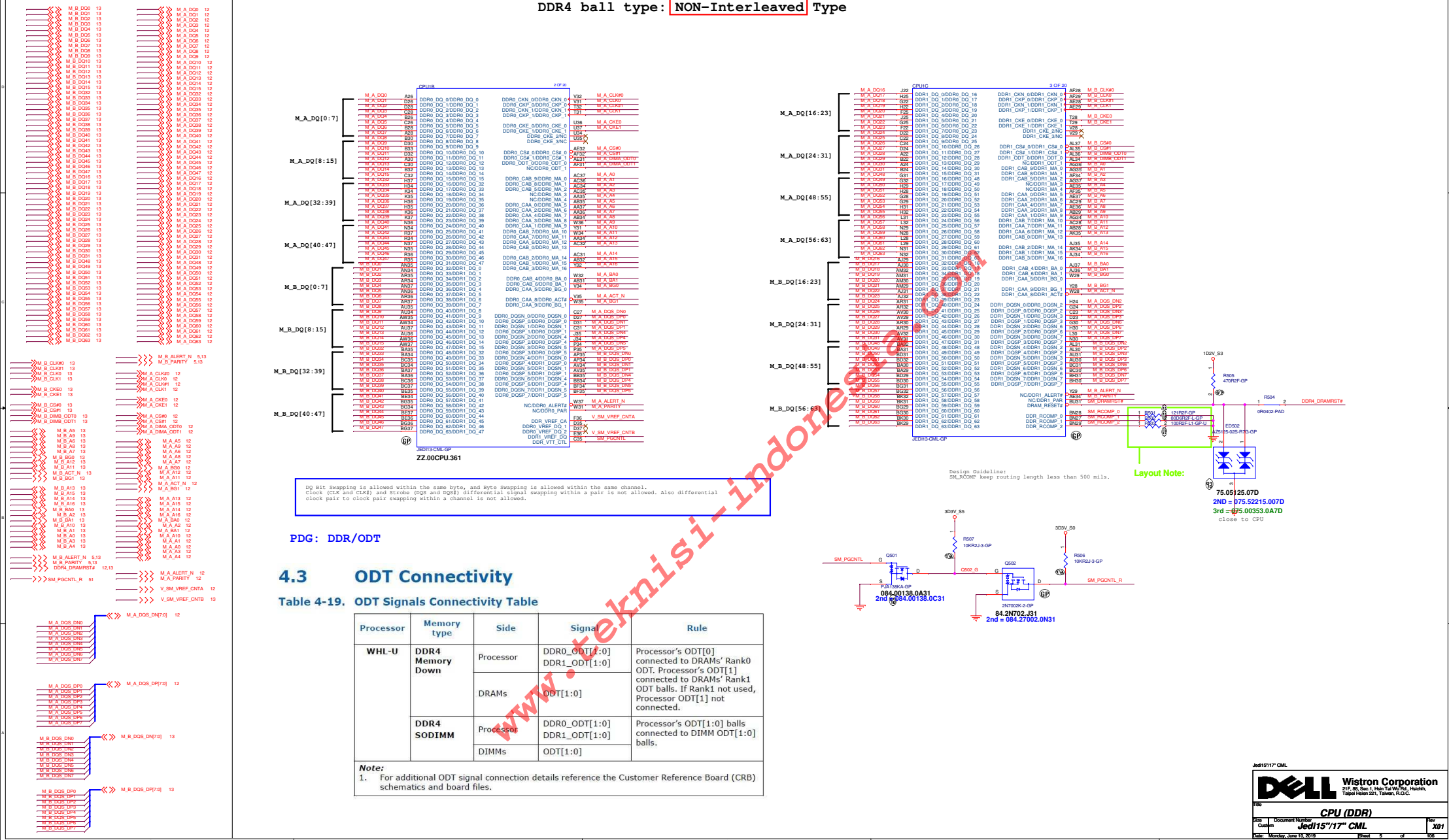
Jedi15/17" CML

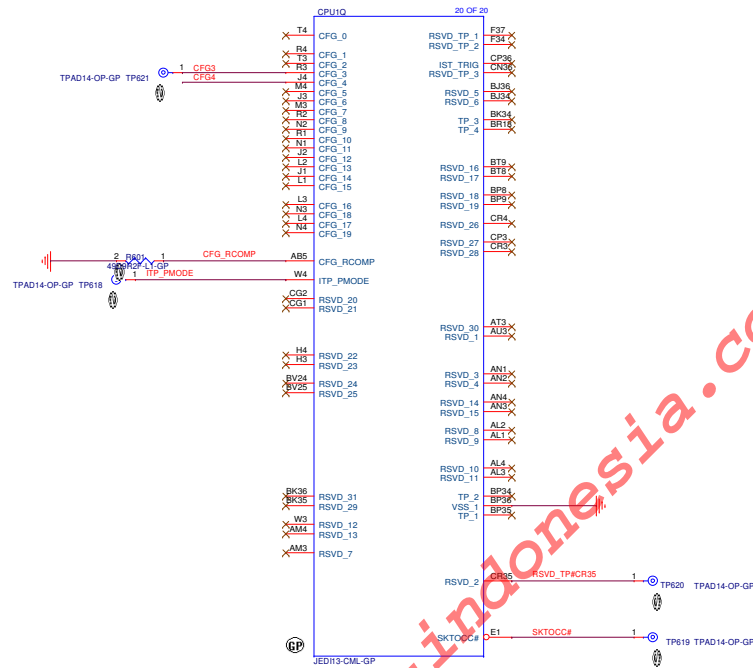
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File: **CPU (DDI/EDP)**

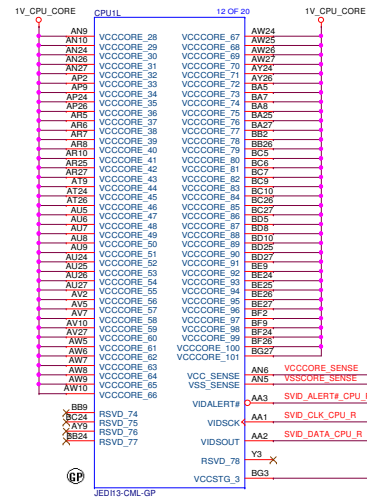
Size: A2 Document Number: **Jedi15"/17" CML** Rev: **X01**

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46 VCCCORE\_SENSE<<<====  
46 VSSCORE\_SENSE<<<====  
  
46 SVID\_DATA\_CPU<<<====  
46 SVID\_CLK\_CPU<<<====  
46 SVID\_ALERT#\_CPU<<<====



1V\_CPU\_CORE

Layout Note:

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Length match<25mil

Layout Note:  
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).  
Route the Alert signal between the Clock and the Data signals.

SVID\_543016:

SVID DATA

SVID CLOCK

SVID ALERT

Figure 7-19. Routing Illustration for SVID Topology

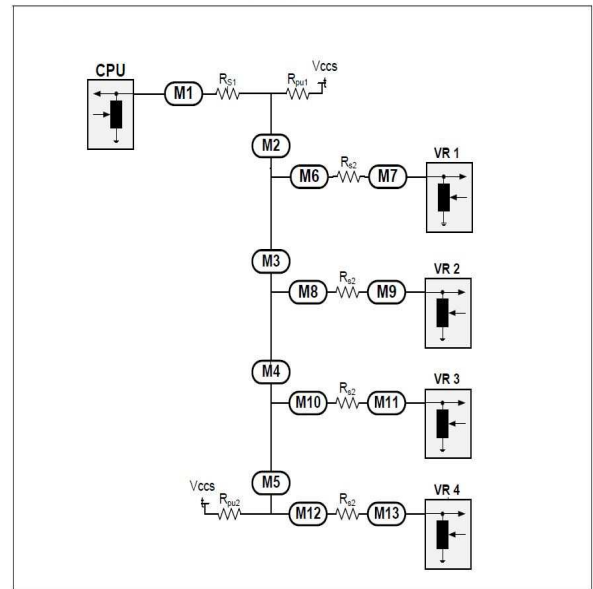


Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals		VIDSOUT, VIDSCK, VIDSALERT#					
VIDSOUT platform resistors		Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω					
VIDSCK platform resistors		Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω					
VIDSALERT# platform resistors		Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω					
Platform resistors tolerances		± 5%					
Route ordering		When routing at minimum spacing route Alert between Data and Clock					
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK		± 100mils					

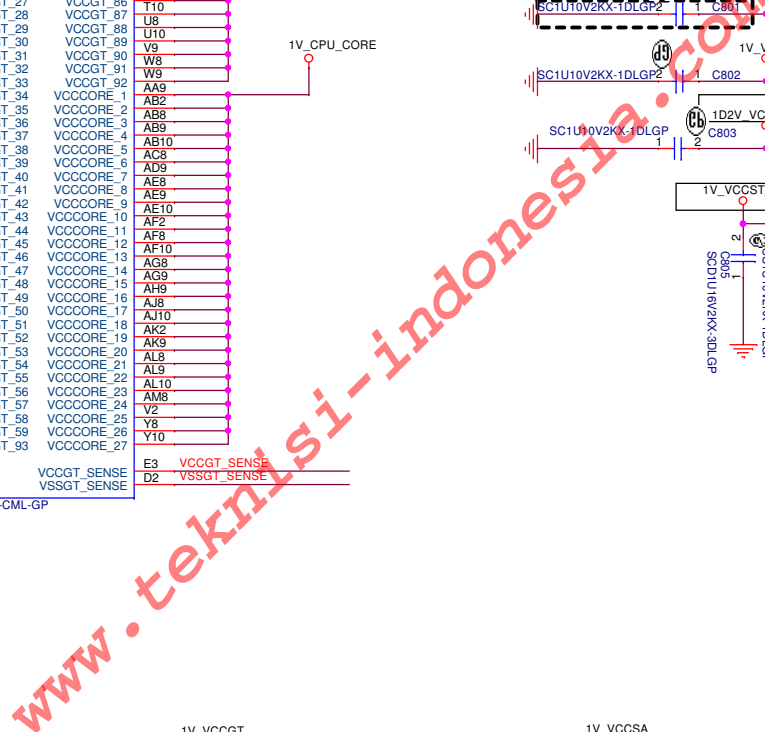
Jedi15/17 CML

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46 VSSSA_SENSE <<< _____
46 VCCSA_SENSE <<< _____

46 VCCGT_SENSE <<< _____
46 VSSGT_SENSE <<< _____

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Title

CPU (RSVD)

Size

A3

Document Number

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Date: Monday, June 10, 2019

Rev

X01

Sheet

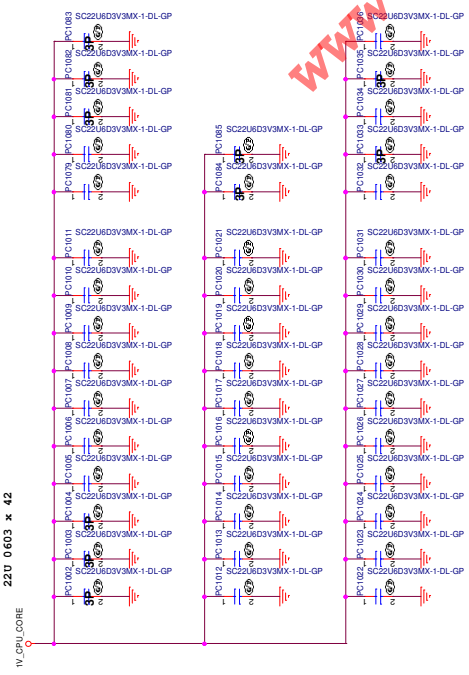
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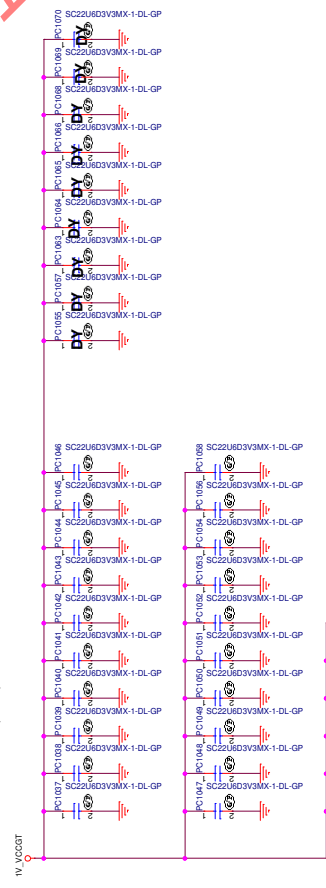
1V\_CPU\_CORE

220 0603 x 42



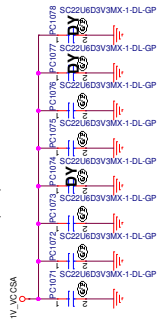
VCCGT

220 0603 x 35 (9 DY)



VCCSA

220 0603 x 8 (3DY)



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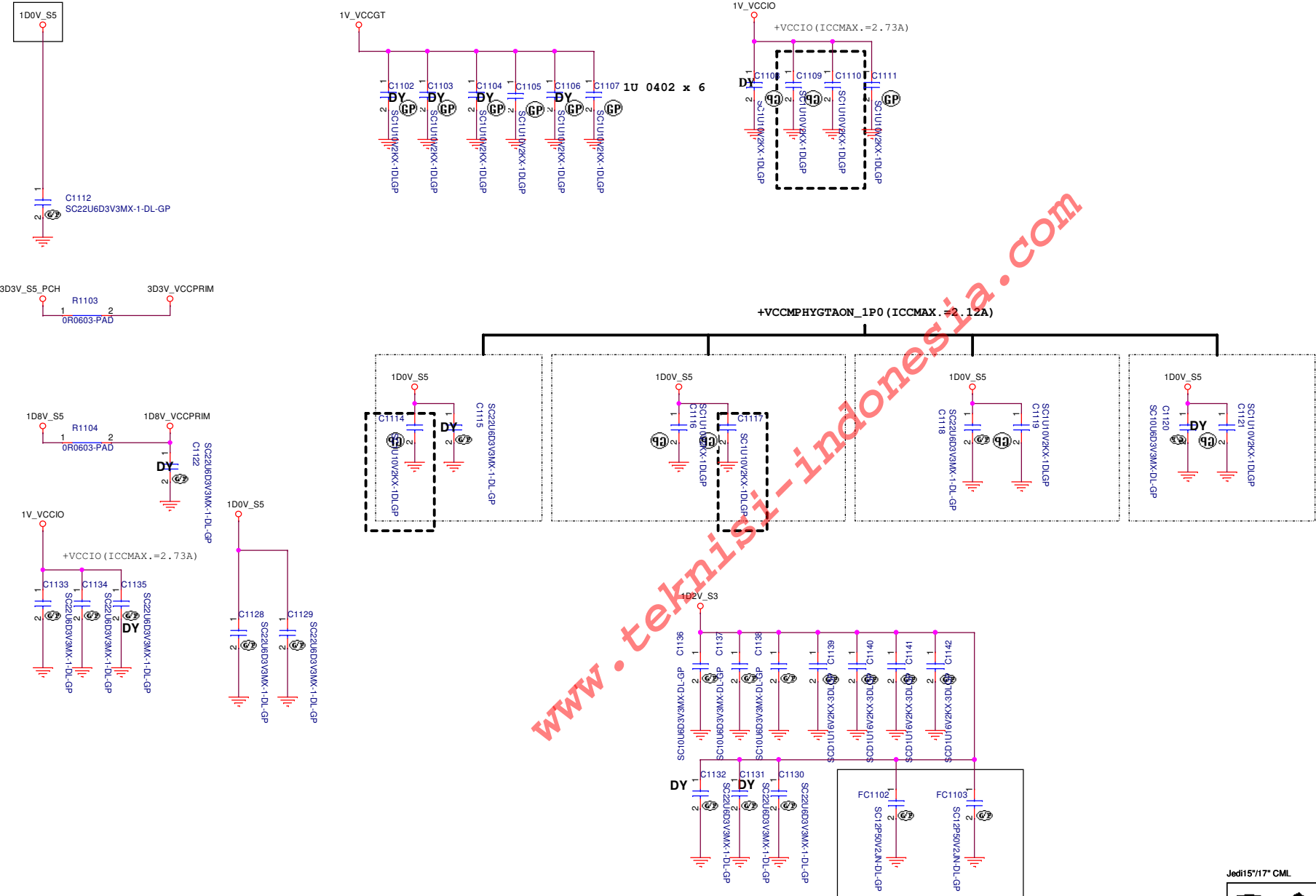
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CPU (Power CAP1)

Doc Number	Rev
Jed1517 CML	A00
DATE: 10/05/2010	BY: 01

Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



Layout Note:

1uF:  
C1174 near N15  
C1180 near K15  
C1173 near AF20  
C1172 near N18  
C1175 near AB19  
22uF :  
C1182 C1184 near N15  
10uF:  
C1176 near N15

RF request 2018/09/28 modify

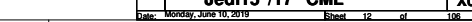
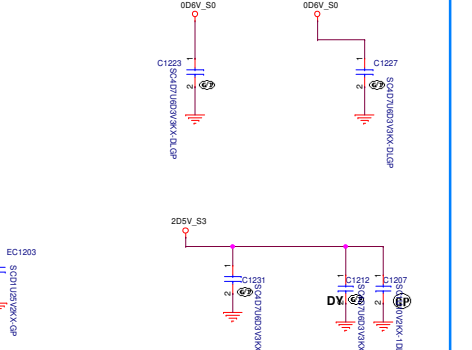
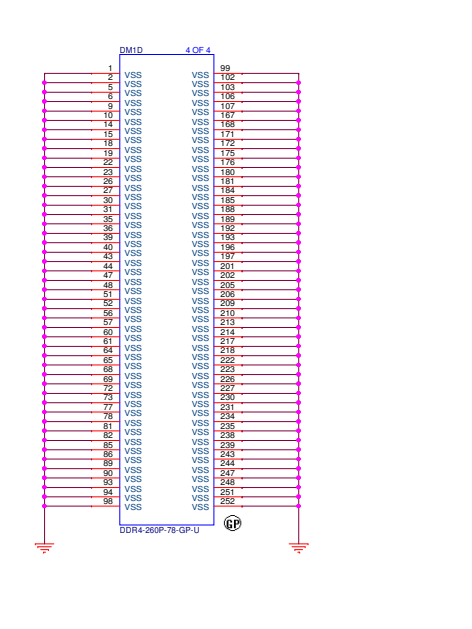
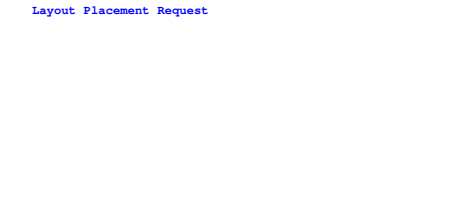
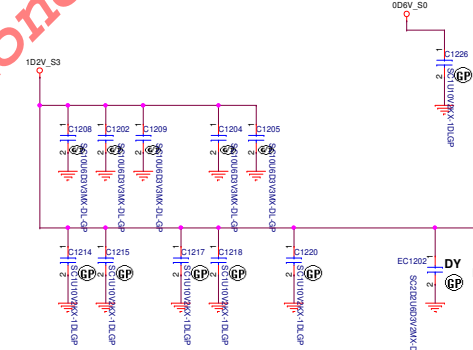
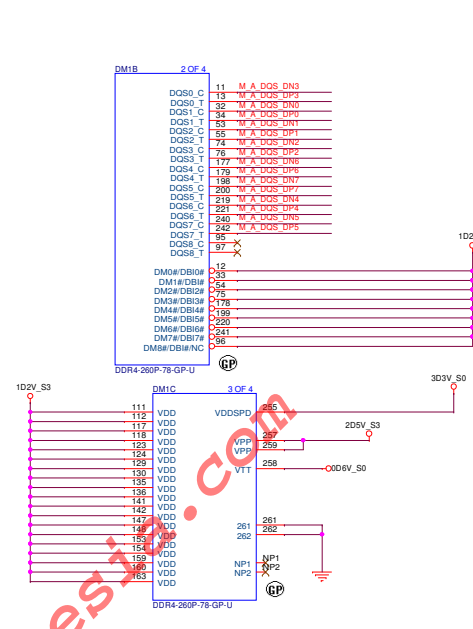
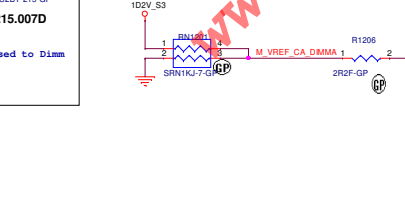
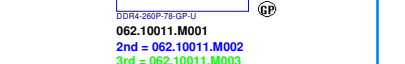
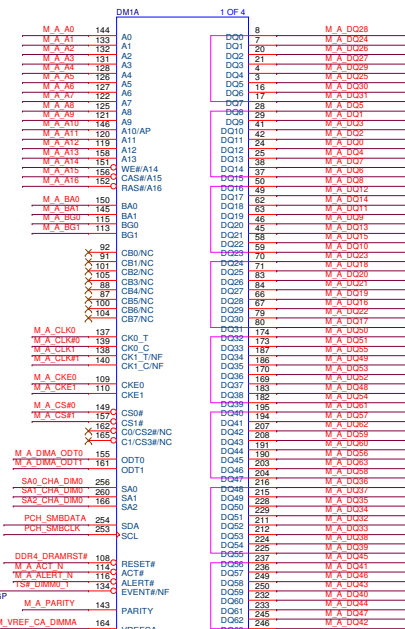
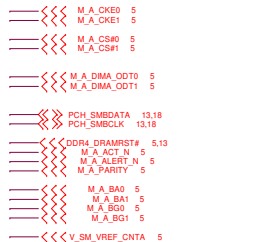
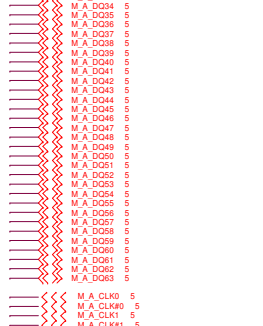
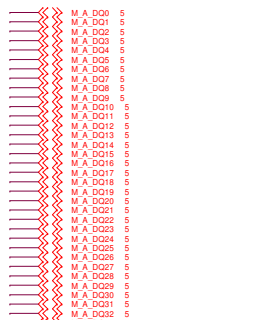
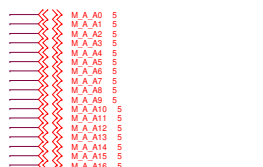
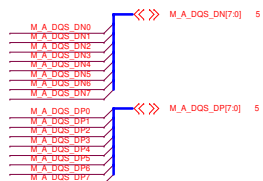
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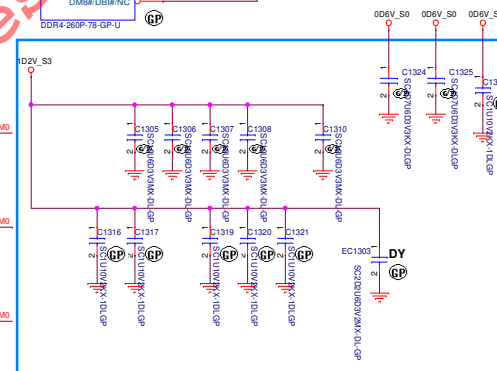
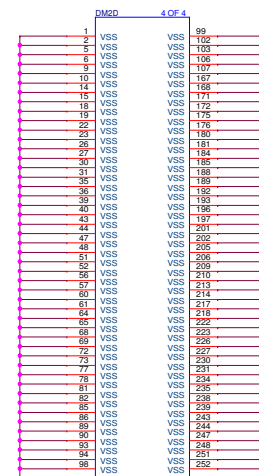
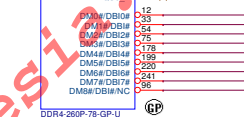
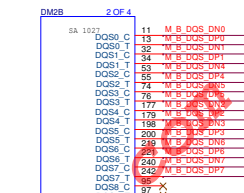
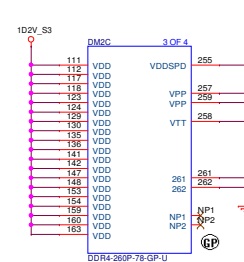
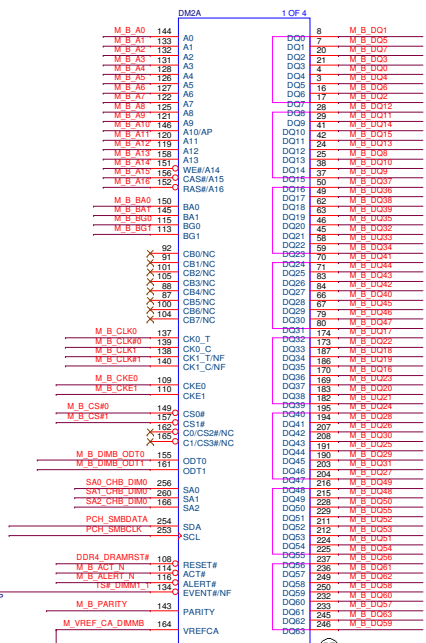
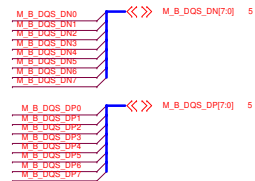
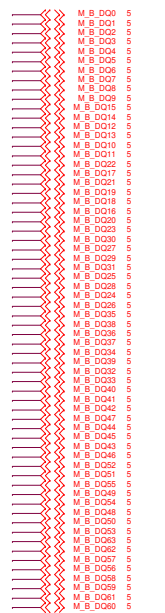
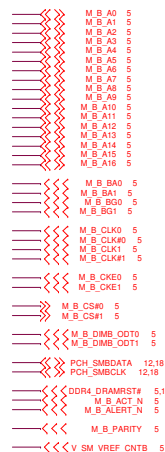
Title: **CPU (Power Cap2)**

Size: A3	Document Number: <b>Jedi15"/17" CML</b>	Rev: <b>X01</b>
Date: Monday, June 10, 2019	Sheet: 11 of 106	

**Main Func = MEMORY**



Main Func = MEMORY



### Layout Placement Request

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Title **DDR (RSVD) (DDR4-CHA1)**

Size A4	Document Number <b>Jedi15"/17" CML</b>	Rev <b>X01</b>
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**Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP**

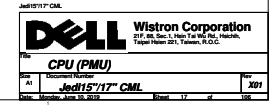
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gem2 #1	USB3.1 Gen1/Gem2 #2	USB3.1 Gen1/Gem2 #3	USB3.1 Gen1/Gem2 #4	USB3.1 Gen1/Gem2 #5	USB3.1 Gen1/Gem2 #6	Pcie #7	Pcie #8	Pcie #9	Pcie #10	Pcie #11	Pcie #12	Pcie #13	Pcie #14	Pcie #15	Pcie #16
	Pcie #1	Pcie #2	Pcie #3	Pcie #4	Pcie #5	Pcie #6	GBE	GBE	GBE	SATA 0	SATA 1a	SATA 1b	GBE	GBE	SATA 1d	SATA 2
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes

### 6.3.1 PCH PCI Express\* Interface Configuration Details

**Figure 6-2. Supported PCH PCI Express\* Link Configurations**

PCH-LP		PCie* Controller #1						PCie* Controller #2						PCie* Controller #3						PCie* Controller #4													
Flex I/O Lane		0		1		2		3		4		5		6		7		8		9		10		11		12		13		14		15	
PCie* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Premium-U	1x6	RP1						RPS						RPS						RP13													
	2x12	RP1						RPS						RPS						RP13													
	2x6	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18	RP19	RP20	RP21	RP22	RP23	RP24	RP25	RP26	RP27	RP28	RP29	RP30	RP31	
	1x12+1x6	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18	RP19	RP20	RP21	RP22	RP23	RP24	RP25	RP26	RP27	RP28	RP29	RP30	RP31	
	0x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16	RP17	RP18	RP19	RP20	RP21	RP22	RP23	RP24	RP25	RP26	RP27	RP28	RP29	RP30	RP31	





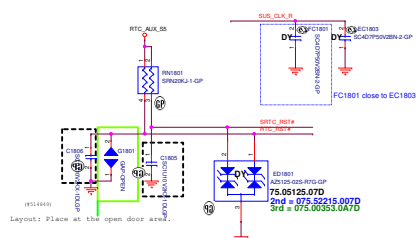
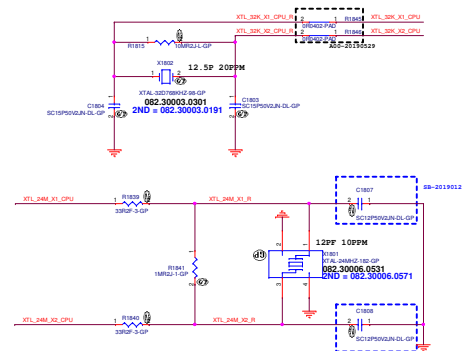
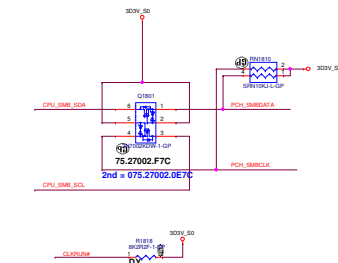
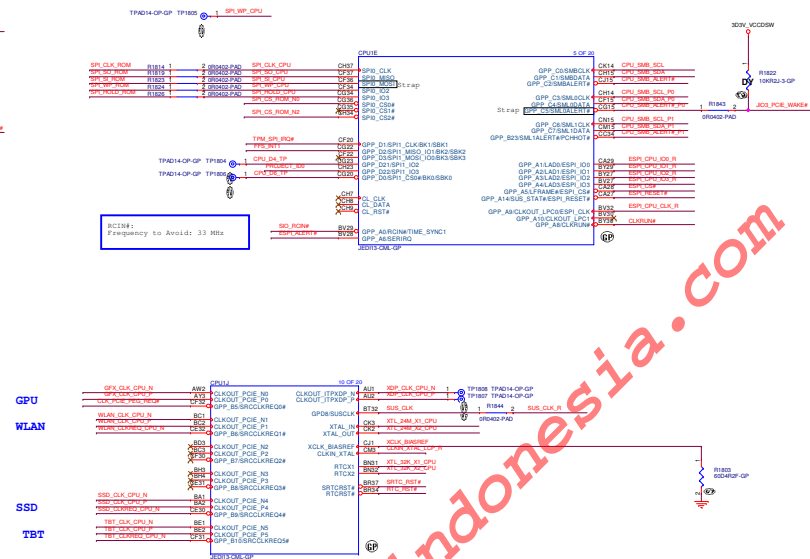
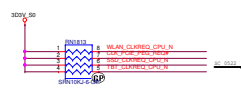


Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

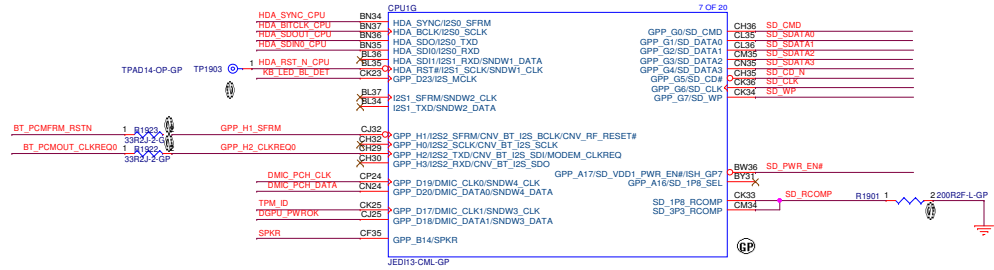
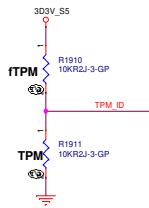
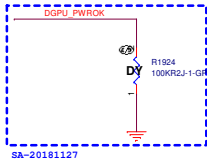
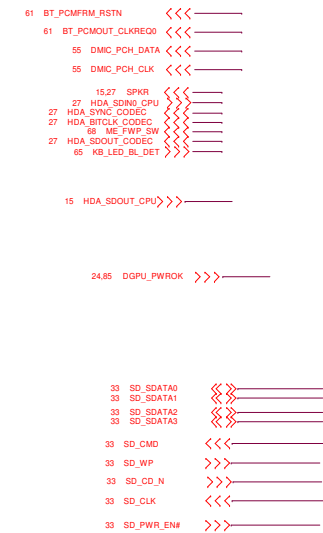
eSPI Enable Strap (eSPI_EN Value (0: LPC, 1: eSPI))	Boot BIOS Strap (BIOS_V value (0: SPI, 1: LPC/eSPI))	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT#/ GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

Signal	Drive	When Sampled	Comment
<b>GP1N_M0S1/ RFP_B12</b>	Boot BIOS Rising edge of PCH_P0VCK		<p>This signal has a weak internal Pull-down.</p> <p>This field determines the destination of access to the BIOS memory region. It can be either BIOS Destination (0 (Jual), Device11, Function), offset BCH, bit 6).</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> <b>Bit 6</b>  <b>Boot BIOS Destination</b>            0 SPI (default)            1 LPC         </div> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after P0VCK# is asserted.</li> <li>If option 1 is selected, BIOS may not be loaded on UEFI, but all platform can be migrated to BIOS on UEFI connected directly to the PCH's SPI bus with a valid destination.</li> <li>Boot BIOS Destination is selected by the option of using Boot BIOS Destination bit and not integrated GPU BIOS Destination bit. If the integrated GPU BIOS Destination bit is set, the integrated GPU BIOS Destination bit will not be used.</li> <li>This signal is in the primary pull.</li> </ol>
<b>SHLGALEF7/ GFP_CS</b>	eSPI or LPC	Rising edge of RSPST#	<p>This signal has a weak internal Pull-down.</p> <ul style="list-style-type: none"> <li>0 - eSPI is selected for CS. (Default)</li> <li>1 - LPC is selected for CS.</li> </ul> <p>The internal Pull-down is disabled after RSPST# is asserted.</p> <ol style="list-style-type: none"> <li>This signal is in the primary pull.</li> </ol>

Main Func = PCH

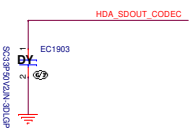
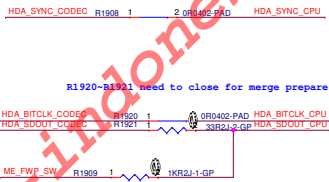


PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable
The internal pull-down is disabled after PLTRST# deasserts	

PCH strap pin:

TOP SWAP OVERRIDE	
HDA_SPKR	High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)
The internal pull-up	



Jed15Y17-CML

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU (HAD/I2S/SD/DMIC)			
Size	Document Number	Rev	
A2	Jed15Y17-CML	X01	
Date	Monday, June 10, 2019	Sheet	19 of 106

```

79,86   G08_FB_EN    <<<_____
55      CPU_IC_SDA_P1 _____
55      CPU_IC_SCL_P1 _____
65,66   CPU_IC_SDA_P0 _____
65,66   CPU_IC_SCL_P0 _____
55      DBC_PANEL_EN _____
68      UART2_C_RXD_DTXD _____
68      UART2_C_CTXD_DRXD _____
24      SID_EXT_WAKE# _____
65      KB_DET#      _____
24,66,69 LID_CL_SIO# _____
55      GSEN2_NT1#   _____
70      GSEN2_NT1    _____

15,25   RTC_DET#     _____
55,70   CPU_IC_SDA_SHD _____
55,70   CPU_IC_SCL_SHD _____
70      FFS_NT2      _____

91      PIRQA#       <<<_____
21      BOARD_ID2    _____
71      PERST_N_CPU  <<<_____

61      CNV_BR1_RSP  _____
15,61   CNV_RGI_DT_R _____
61      CNV_BR1_DT_R _____
61      CNV_RGI_RSP  _____

76      G04_HOLD_RST# _____
79      GPU_EVENT#   _____

86      GPU_PWR_EN   _____

15      NRB_BIT      _____

15      GPP_B22_GSPI_MOSI _____

24      NB_MODE#     _____

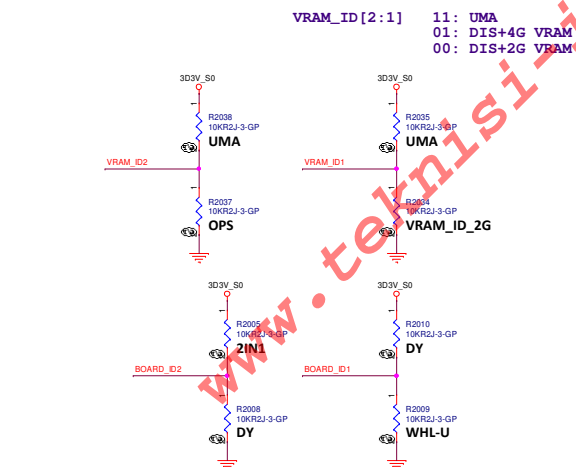
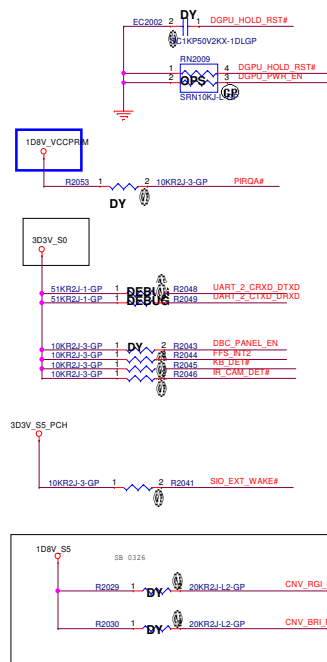
24,66,69 LID_CL_SIO_TAW# _____

24      ISH_TABLE_MODE# _____

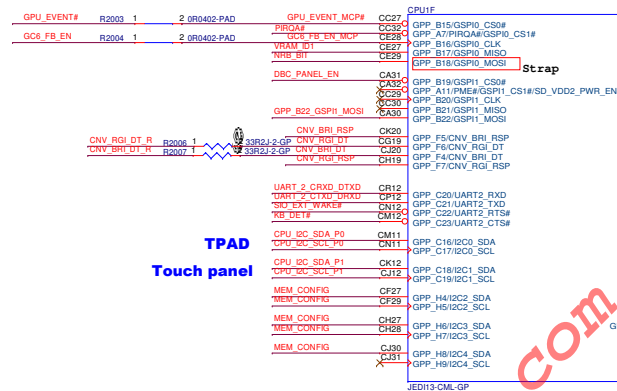
71      TBT_PCIE_WAKE# _____

4      IR_CAM_DET#   _____

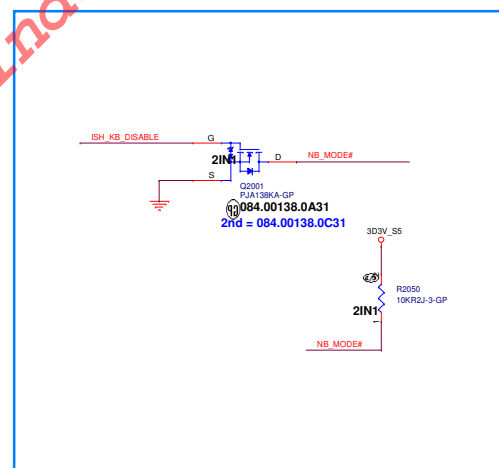
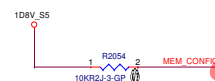
```



MODEM AND NFC REFERENCE CLOCK SOURCE SELECT  
1 = CLKIN\_XTAL\_LCP  
0 = XTAL\_IN  
PCH HAS INTERNAL 20K PU



**TPAD**  
**Touch panel**



PCH strap pin: NRB BIT

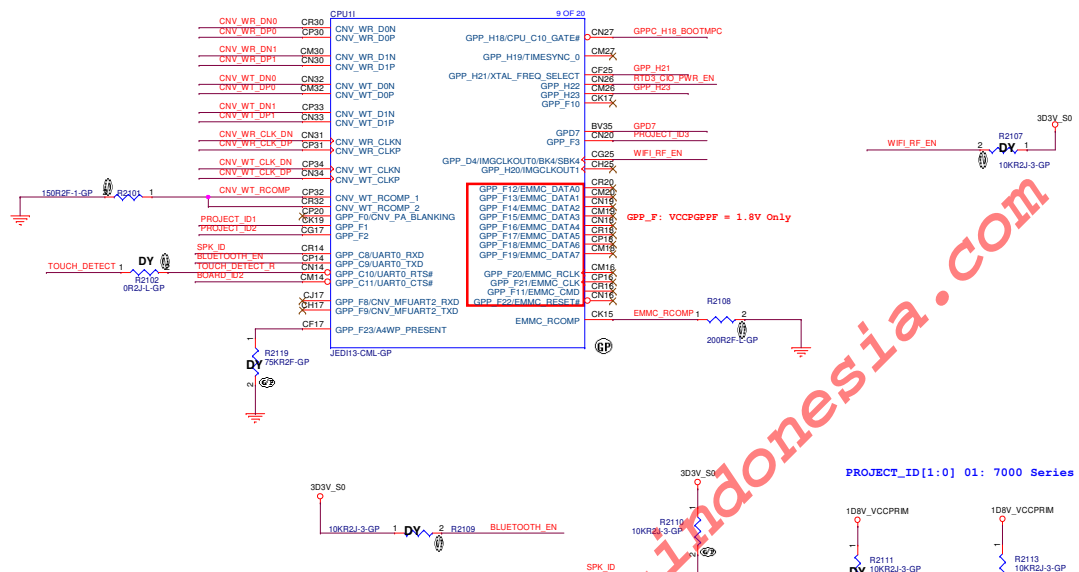
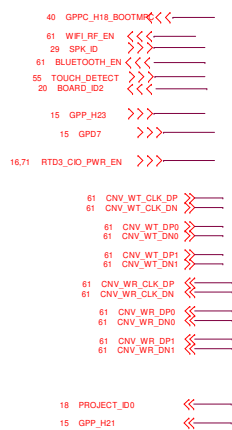
<b>No Reboot</b>	Sampled at rising edge of PCH_PWROK
<b>GSPI0_MOSI / GPP_B18</b>	<p>0 = Disable "No Reboot" mode.</p> <p>1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p>

The signal has a weak internal pull-down.

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

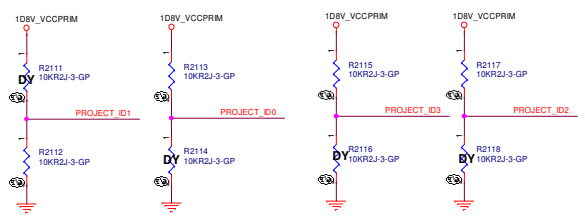
Jedi15<sup>+/17</sup> CML

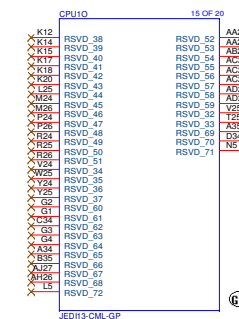
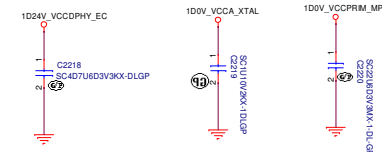




PROJECT\_ID[1:0] 01: 7000 Series

PROJECT\_ID[3:2] 11: Inspiron



[illegible]

Main Func = PCH

CPU1R 17 OF 20			
CR34	VSS_342	VSS_330	BL7
BY5	VSS_351	VSS_307	AE7
CP45	VSS_351	VSS_345	BM33
CM37	VSS_371	VSS_354	CM5
CK37	VSS_381	VSS_364	AE7
AW17	VSS_381	VSS_374	BM35
CM11	VSS_401	VSS_384	AE9
BD6	VSS_411	VSS_302	BM36
AV4	VSS_421	VSS_308	CM14
BS4	VSS_360	VSS_315	AE7
ES6	VSS_370	VSS_305	BM37
A4	VSS_380	VSS_329	CM17
AE54	VSS_350	VSS_334	AF27
AE36	VSS_400	VSS_344	BM37
AF25	VSS_410	VSS_353	CM21
AG24	VSS_420	VSS_363	ES1
AG26	VSS_428	VSS_373	BN7
AH24	VSS_434	VSS_383	CM25
AH25	VSS_296	VSS_301	AF10
B2	VSS_350	VSS_307	CM29
BC6	VSS_359	VSS_314	AF35
CS6	VSS_369	VSS_321	BP15
CS7	VSS_379	VSS_329	AF36
CM11	VSS_389	VSS_335	CM5
CM2	VSS_399	VSS_343	AF7
CM37	VSS_409	VSS_352	BP25
CF2	VSS_419	VSS_362	CM9
DI1	VSS_427	VSS_416	AG10
A32	VSS_433	VSS_425	BP3
F33	VSS_341	VSS_432	CM9
AT	VSS_349	VSS_294	CP11
BL7	VSS_358	VSS_300	BP42
CL36	VSS_368	VSS_306	CP11
A36	VSS_378	VSS_313	AH27
BK10	VSS_388	VSS_320	BP33
C14	VSS_398	VSS_327	CP13
AB27	VSS_408	VSS_334	AH28
BM2	VSS_418	VSS_405	BP5
CK1	VSS_426	VSS_415	CP15
AB3	VSS_333	VSS_424	AH29
BK28	VSS_340	VSS_431	BP7
AB30	VSS_348	VSS_293	CP19
BK3	VSS_357	VSS_299	AH30
CK4	VSS_367	VSS_305	CP21
AB33	VSS_377	VSS_312	AH31
BK33	VSS_387	VSS_319	BP16
CK7	VSS_397	VSS_326	CP27
AB39	VSS_407	VSS_334	AH33
BK4	VSS_417	VSS_404	BP25
CL12	VSS_305	VSS_414	AH35
AK4	VSS_302	VSS_423	CP17
BK7	VSS_309	VSS_430	AJ25
CA13	VSS_347	VSS_292	BT15
AB7	VSS_356	VSS_298	AJ28
BL25	VSS_366	VSS_304	BT16
CM17	VSS_376	VSS_311	CP2
AC10	VSS_386	VSS_318	AJ7
BL28	VSS_396	VSS_323	CP2
CM21	VSS_406	VSS_330	AK5
AC27	VSS_416	VSS_403	CR36
BL29	VSS_324	VSS_413	AK53
CM25	VSS_331	VSS_422	D21
AC30	VSS_338	VSS_429	AK58
BL30	VSS_346	VSS_291	BT25
CM29	VSS_355	VSS_297	CS2
BL31	VSS_365	VSS_303	CS2
CM31	VSS_375	VSS_310	BT28
AD33	VSS_385	VSS_312	AL28
BL32	VSS_395	VSS_362	BT33
CM33	VSS_405	VSS_366	D5
AD35	VSS_316	VSS_402	AL29
VSS_323	VSS_323		

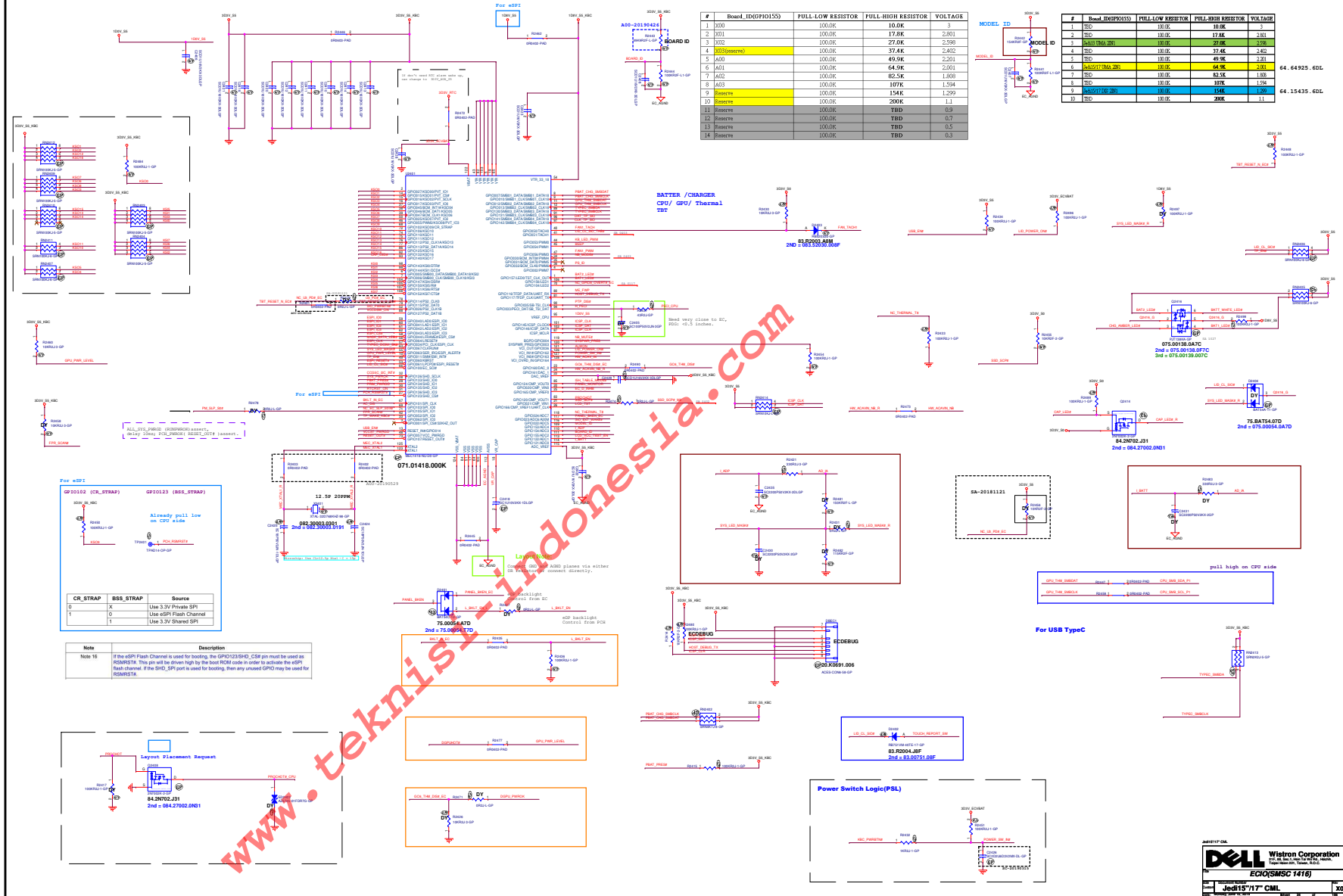
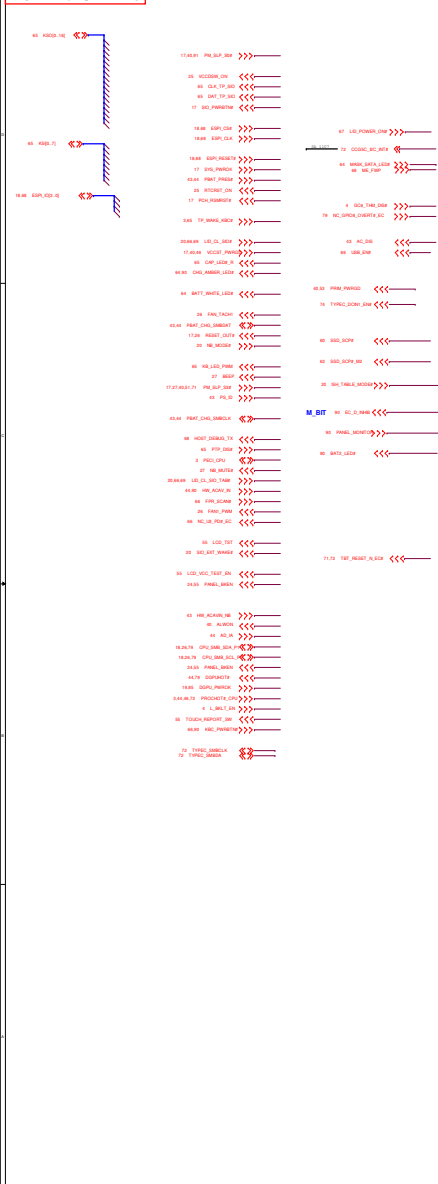
JED13-CML-GP  
ZZ.00CPU.361

CPU1S 18 OF 20			
BT35	VSS_277	VSS_180	J16
DB	VSS_290	VSS_189	AE7
AL32	VSS_156	VSS_186	BY26
BT36	VSS_165	VSS_245	J21
DB	VSS_172	VSS_251	AE7
AL	VSS_208	VSS_270	BY23
DB	VSS_217	VSS_284	CM2
AM17	VSS_227	VSS_151	AV28
BU11	VSS_238	VSS_161	BY35
E23	VSS_250	VSS_169	CM23
AM23	VSS_263	VSS_178	AV3
E27	VSS_273	VSS_179	BY36
BM37	VSS_289	VSS_182	J36
BU23	VSS_299	VSS_192	AV33
E29	VSS_315	VSS_203	AV38
AM35	VSS_164	VSS_244	J8
BU24	VSS_200	VSS_256	AV38
E31	VSS_207	VSS_266	CM2
BU25	VSS_216	VSS_283	K21
E33	VSS_228	VSS_199	K21
AN25	VSS_237	VSS_161	AV4
BU7	VSS_249	VSS_168	K22
E35	VSS_262	VSS_171	AV6
AN28	VSS_275	VSS_178	CM5
AF35	VSS_282	VSS_172	K24
BU11	VSS_154	VSS_232	AV8
F12	VSS_194	VSS_243	CM9
AN29	VSS_199	VSS_252	CM5
AN30	VSS_206	VSS_260	AW28
F18	VSS_215	VSS_263	C33
AN31	VSS_225	VSS_143	K27
BU3	VSS_236	VSS_159	AW29
F21	VSS_248	VSS_161	K27
AN7	VSS_261	VSS_173	K28
AN31	VSS_274	VSS_211	AW3
AN8	VSS_287	VSS_221	CM9
AN8	VSS_189	VSS_231	K29
BY33	VSS_193	VSS_241	AW30
F24	VSS_198	VSS_254	CA11
BU4	VSS_205	VSS_261	K3
F3	VSS_214	VSS_281	AW31
AP3	VSS_224	VSS_146	CA15
BU11	VSS_235	VSS_154	K30
F4	VSS_247	VSS_160	AY33
AP33	VSS_260	VSS_203	CA22
BU15	VSS_273	VSS_211	K31
G21	VSS_185	VSS_229	AY35
AP36	VSS_188	VSS_239	K32
G27	VSS_192	VSS_241	BT2
AP4	VSS_197	VSS_253	K4
G33	VSS_204	VSS_266	BT5
AR28	VSS_213	VSS_280	K4
Q35	VSS_223	VSS_147	CA25
Q36	VSS_234	VSS_157	BT8
AT35	VSS_246	VSS_196	CM11
BU24	VSS_259	VSS_202	J27
G39	VSS_272	VSS_213	B21
AT36	VSS_286	VSS_219	L31
H21	VSS_153	VSS_229	B23
AT38	VSS_163	VSS_240	L35
BU7	VSS_171	VSS_252	B25
H27	VSS_177	VSS_265	CM18
BY11	VSS_181	VSS_276	L38
BY11	VSS_184	VSS_146	B27
AL10	VSS_187	VSS_159	CM18
BY15	VSS_191	VSS_195	L6
H9	VSS_258	VSS_201	CM9
BU25	VSS_271	VSS_209	CM9
BY22	VSS_285	VSS_216	K25
J12	VSS_152	VSS_226	AL28
AU29	VSS_162	VSS_239	CM30
J15	VSS_170	VSS_251	K27
J15	VSS_176	VSS_264	CM24
	VSS_278		

JED13-CML-GP  
ZZ.00CPU.361

CPU1T 19 OF 20			
NE	VSS_66	VSS_99	CF23
CB7	VSS_73	VSS_106	BE30
P10	VSS_79	VSS_115	CF24
BE5	VSS_84	VSS_126	BY10
CB33	VSS_89	VSS_139	BE31
P23	VSS_95	VSS_8	CP3
BT	VSS_102	VSS_19	W27
CB4	VSS_110	VSS_29	CF4
P33	VSS_120	VSS_83	W27
BE9	VSS_132	VSS_87	BP3
CB7	VSS_145	VSS_92	CM33
P36	VSS_14	VSS_98	W7
BA10	VSS_25	VSS_105	BP33
CM11	VSS_35	VSS_114	CM7
P4	VSS_44	VSS_125	BP36
BA28	VSS_52	VSS_138	CM2
P7	VSS_59	VSS_7	BF4
BA3	VSS_65	VSS_16	CF31
CB20	VSS_72	VSS_77	CF31
R27	VSS_78	VSS_82	BC25
BE3	VSS_131	VSS_86	CM9
CM25	VSS_144	VSS_91	BC28
VSS_13	VSS_151	VSS_97	CM9
R28	VSS_24	VSS_104	CM11
BE33	VSS_34	VSS_113	CM9
CM28	VSS_43	VSS_124	CM14
R29	VSS_51	VSS_137	CM9
BE36	VSS_58	VSS_141	CM9
R30	VSS_64	VSS_70	W7
BE4	VSS_71	VSS_74	BP29
CM7	VSS_119	VSS_81	CM2
R31	VSS_130	VSS_85	BP32
BC25	VSS_143	VSS_96	CM28
CM11	VSS_12	VSS_96	BP33
T27	VSS_23	VSS_103	CM33
CM12	VSS_33	VSS_112	BP35
T30	VSS_42	VSS_123	CM35
BC28	VSS_50	VSS_136	BP19
CM14	VSS_57	VSS_5	BP16
T33	VSS_63	VSS_17	BY18
R35	VSS_109	VSS_28	BP19
BC32	VSS_118	VSS_38	CM16
CM24	VSS_128	VSS_47	CM16
T36	VSS_142	VSS_55	CM14
CM25	VSS_11	VSS_62	BP22
BC4	VSS_22	VSS_69	BP22
CM33	VSS_32	VSS_75	CM20
CM33	VSS_41	VSS_86	BT12
CM33	VSS_49	VSS_135	BP12
CM33	VSS_56	VSS_4	CM24
CM33	VSS_101	VSS_16	CM24
CM33	VSS_117	VSS_37	CM24
CM33	VSS_128	VSS_46	BP7
CM33	VSS_141	VSS_54	BP4
CM33	VSS_10	VSS_61	BP4
CM33	VSS_21	VSS_68	AW4
CM33	VSS_31	VSS_74	BP4
CM33	VSS_40	VSS_122	BP4
CM33	VSS_48	VSS_134	BP4
CM33	VSS_94	VSS_3	BP4
CM33	VSS_100	VSS_15	BP4
CM33	VSS_107	VSS_26	BP4
CM33	VSS_116	VSS_36	BP4
CM33	VSS_127	VSS_45	BP4
CM33	VSS_140	VSS_53	BP4
CM33	VSS_9	VSS_64	BP4
CM33	VSS_26	VSS_67	BP4
CM33	VSS_36	VSS_71	BP4
CM33	VSS_88	VSS_133	BP4
CM33	VSS_93	VSS_2	BP4

JED13-CML-GP  
ZZ.00CPU.361



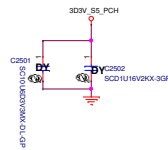
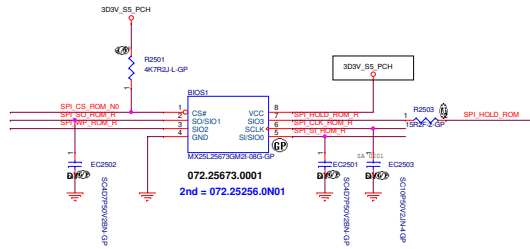
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**Main Func = SPI Flash**

SPI Flash ROM( 32M ) for PCH

18 SPI\_CS\_ROM\_N0 >>>  
15,18 SPI\_HOLD\_ROM <<<  
24 RTCRST\_ON >>>  
52,53 3V\_SV\_DSW\_OK <<<  
18,91 SPI\_SO\_ROM <<<  
15,18 SPI\_SO\_ROM <<<  
18,91 SPI\_SO\_ROM <<<  
15,18,91 SPI\_SO\_ROM <<<  
15,20 RTC\_DET# <<<  
24 VCCDSW\_ON >>>  
17,45 3V\_SV\_PWRGD >>>

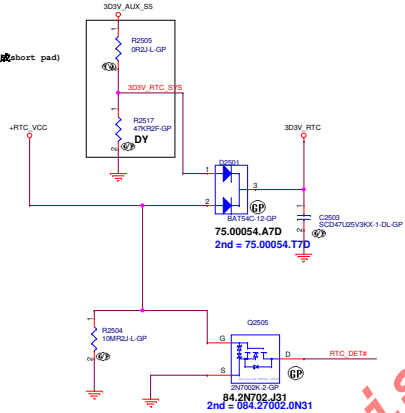


Source	QUAD/DUAL fast read	DUAL fast read	SFDP
772.25128.0851	0	0	0
772.25127.0001	0	0	0
772.25128.0045	0	0	0



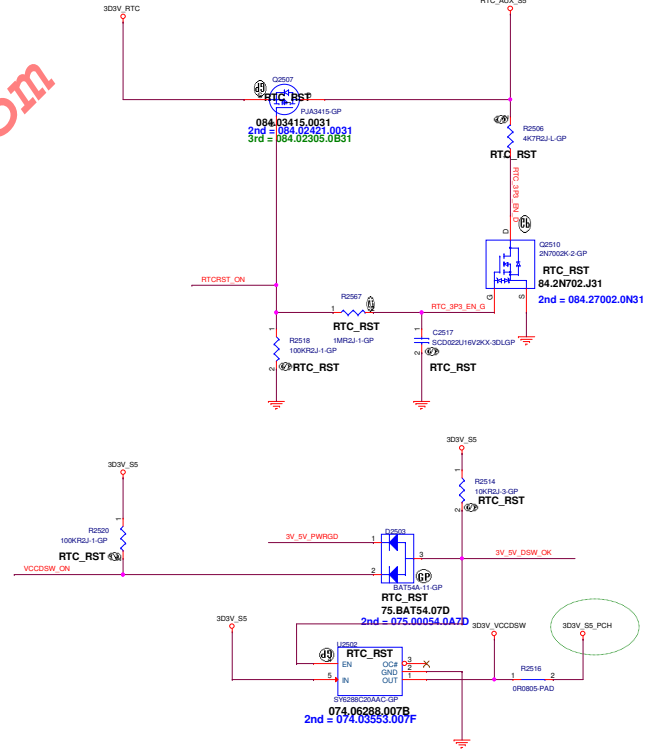
**Main Func = RTC**

(R2505 盡量換不要改成short pad)



**29.2.1 VCCRTC External Circuit**

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



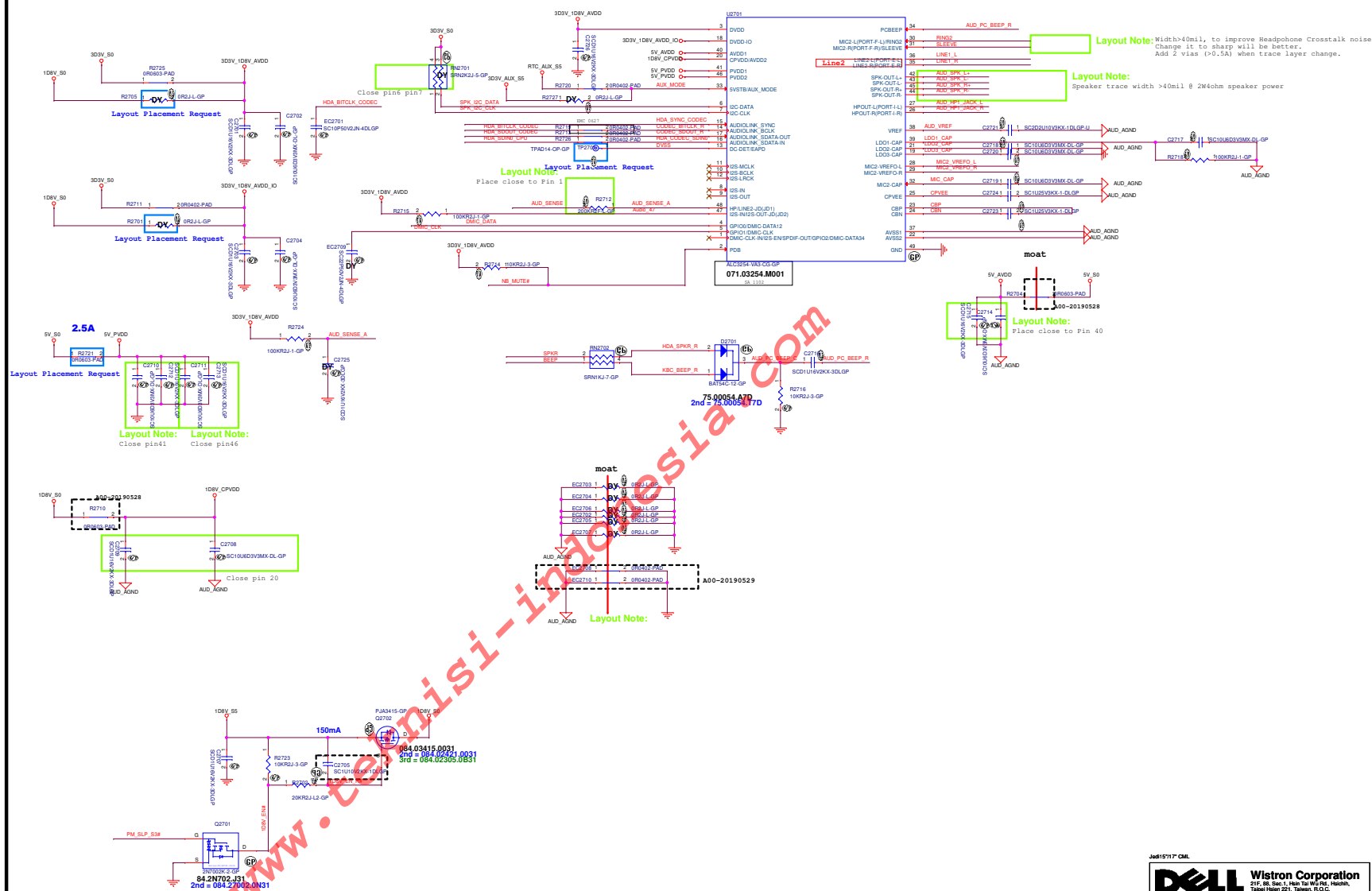


**Main Func = Audio**

```

19  HDA_SYNC_CODEC >>>
19  HDA_SOUT_CODEC >>>
19  HDA_BTLCN_CODEC >>>
55  DMIC_DATA <<<
68  AUD_SENSE <<<
19  HDA_SOUND_CPU <<<
55  DMIC_CLK <<<
24  BEEP <<<
29.68  RING2 >>>
15.18  SPKR >>>
29  LINE1_L >>>
29  LINE1_R >>>
24  NB_MUTE# >>>
29  AUD_SPK_L+ <<<
29  AUD_SPK_L- <<<
29  AUD_SPK_R+ <<<
29  AUD_SPK_R- <<<
29  AUD_HP1 JACK_L <<<
29  AUD_HP1 JACK_R <<<
29  MIC2_VREF0_L <<<
29  MIC2_VREF0_R <<<
29.66  SLEEP >>>
17.40,51.71  PM_PL_S3# >>>

```



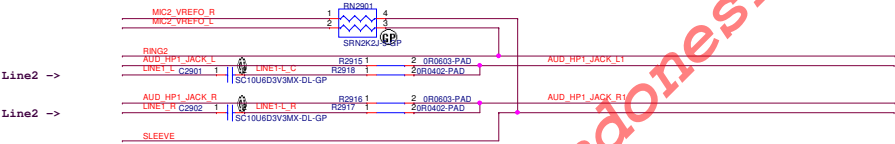
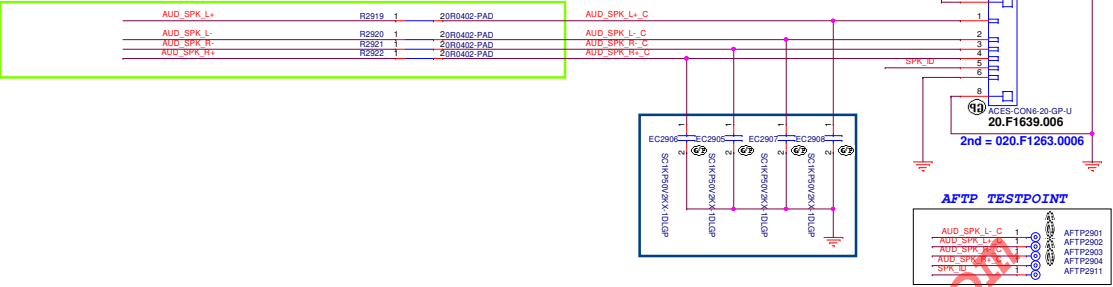
(Blanking)

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Main Func = Audio


21 SPK\_ID <<<—  
27 AUD\_SPK\_L+ >>>—  
27 AUD\_SPK\_L- >>>—  
27 AUD\_SPK\_R- >>>—  
27 AUD\_SPK\_R+ >>>—  
  
27 MIC2\_VREFO\_R >>>—  
27 MIC2\_VREFO\_L >>>—  
27,29,66 RING2 <<<—  
27 LINE1\_L >>>—  
  
27 LINE1\_R >>>—  
  
27,29,66 SLEEVE <<<—  
  
  
27 AUD\_HP1\_JACK\_L >>>—  
27 AUD\_HP1\_JACK\_R >>>—  
  
27,66 AUD\_SENSE >>>—  
  
66 AUD\_HP1\_JACK\_L1 <<<—  
27,29,66 RING2 <<<—  
27,29,66 SLEEVE <<<—  
66 AUD\_HP1\_JACK\_R1 <<<—

Layout Note:  
Speaker trace width >40mil @ 2W4ohm speaker power



www.teknisi-indonesia.com

Jedi15"/17" CML



Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio (RSVD)

Size  
A3

Document Number  
Jedi15"/17" CML


Rev  
X01

Date: Monday, June 10, 2019

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(Blanking)

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Jedi15Y17" CML	
	
Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
LAN (RSVD)	
Size	Document Number
A2	Jedi15"/17" CML
Date	Monday, June 10, 2019
Sheet	31 of 106
Rev	X01

(Blanking)

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Title

**LAN (RSVD) (RJ45+Transfor**

Size  
A3

Document Number

**Jedi15"/17" CML**

Rev

**X01**

Date: Monday, June 10, 2019


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Title


**USB (RSVD) (USB2.0 CONN)**

Size	Document Number	Rev
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Title

USB (RSVD) (USB3.0 Conn)

SizeDocument Number


Jedi15"/17" CML

RevX01

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Title


**USB (RSVD) (USB Charger)**

Size	Document Number	Rev
A3	<b>Jedi15"/17" CML</b>	<b>X01</b>

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>USB (RSVD) (PCIE to USB3.0)</b>		
Size	Document Number	Rev
A4	<b>Jedi15"/17" CML</b>	<b>X01</b>
Date: Monday, June 10, 2019		Sheet 37 of 106

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Jedi15"/17" CML

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b><i>USB (RSVD) (USB3.0 Redriver)</i></b>		
Size	Document Number	Rev
A4	<b><i>Jedi15"/17" CML</i></b>	<b><i>X01</i></b>
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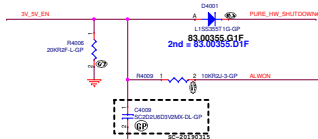
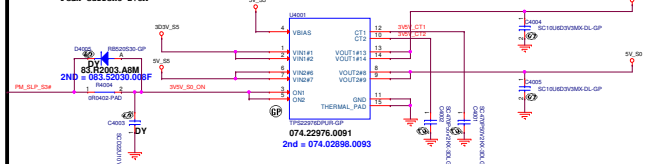
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Jedi15Y17" CML		
		
Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Sequence (RSVD)		
Size A2	Document Number Jedi15Y17" CML	Rev X01
Date: Monday, June 10, 2019		
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17.27.51.71 PM\_SLP\_S0M >>>  
51 VCCST\_PWRGD >>>  
17.28.46 VCCST\_PWRGD <<<  
40 3V\_5V\_EN <<<  
24 ALWON >>>  
25 PURE\_HV\_SHUTDOWNM >>>  
17.28.58 PM\_SLP\_S0M >>>  
52 10V\_V5\_PWRGD >>>  
24.53 PMAL\_PWRGD >>>  
17.25.45 3V\_5V\_PWRGD >>>  
17.28.51 PM\_SLP\_S0M >>>  
21 GPMCH\_HV\_BOOTM <<<

5V\_S0 Consumption  
Peak current 5A  
3D3V\_S0  
3D3V\_S0 Consumption  
Peak current 2.5A

## ROSA Run Power



## EOPIO and EDRAM

## +V\_EDRAM\_VR

Voltage = 1.0 V  $\pm$  50 mV  
Imax = 3.2 A  
TRISE = 240 us

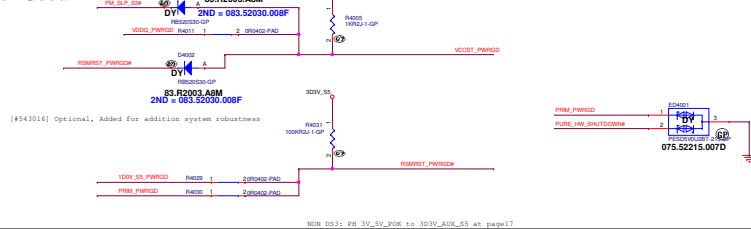
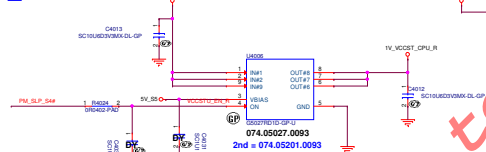
## +V\_EOPIO\_VR

Voltage = 1.0 V  $\pm$  50 mV  
Imax = 2.8 A  
TRISE = 240 us

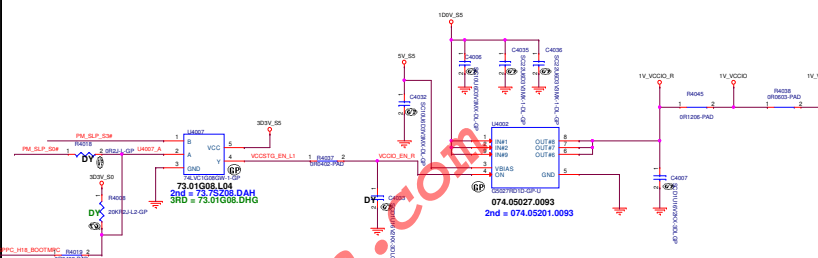
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

## MANAGEMENT RAIL POWER GENERATION

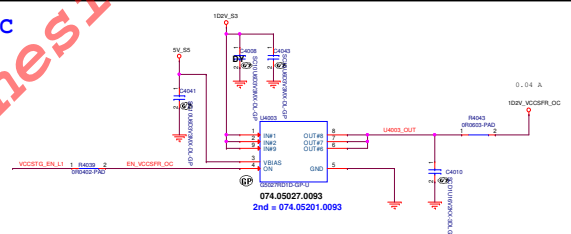
## VCCST\_CPU



## +VCCIO/+VCCSTG



## 1D2V\_VCCSFR\_OC




## +V1.8S0




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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Sequence (RSVD) (DS3/S0ix)</b>		
Size A4	Document Number <b>Jedi15"/17" CML</b>	Rev <b>X01</b>
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Jedi15Y17" CML

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>INT IO (RSVD)</b>		
Size A2	Document Number <b>Jedi15"/17" CML</b>	Rev <b>X01</b>
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24 HW\_ACAVIN\_NB <<<—

24 PS\_ID <<<—

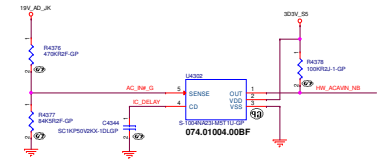
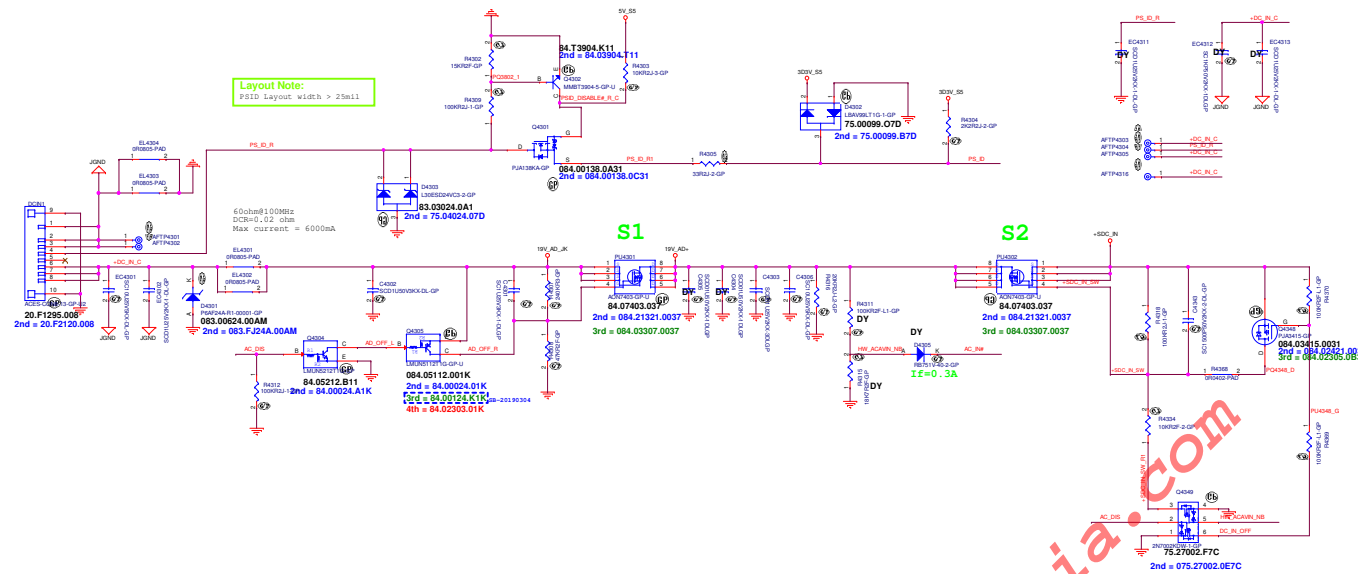
17.44 AC\_IN# <<<—

24 AC\_DIS <<<—

24.44 PBAT\_OHG\_SMBCLK <<<—

24.44 PBAT\_OHG\_SMBRST <<<—

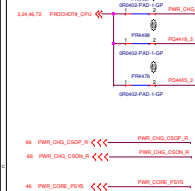
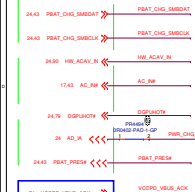
24.44 PBAT\_PRES# <<<—

[illegible]

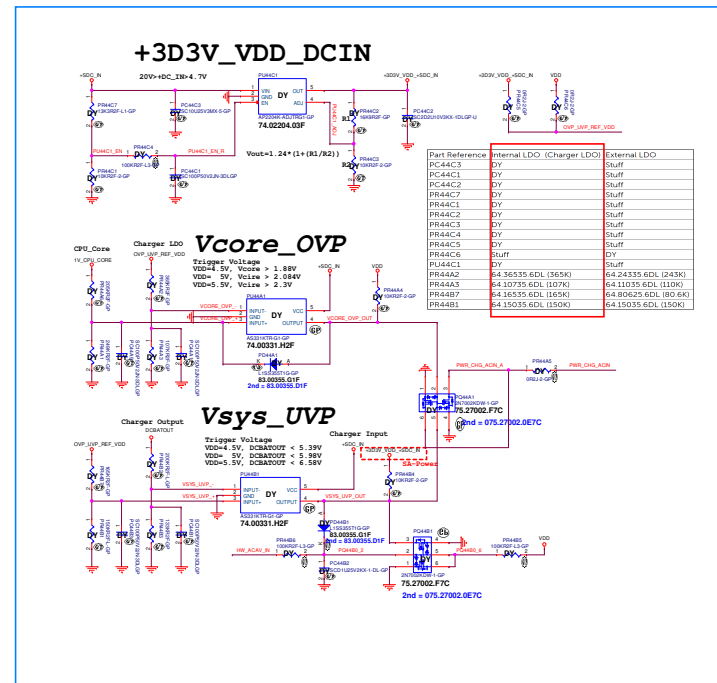
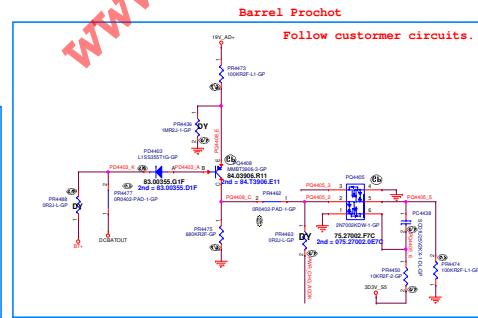
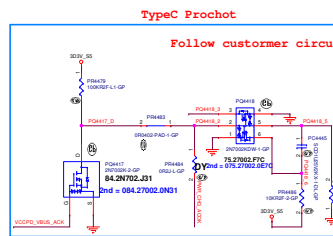
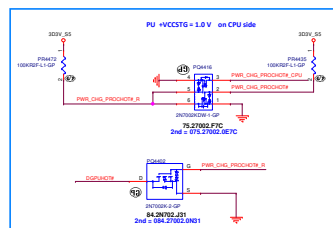
## ISL9538H For Charger

## OFFPAGE

EE needs check is !!

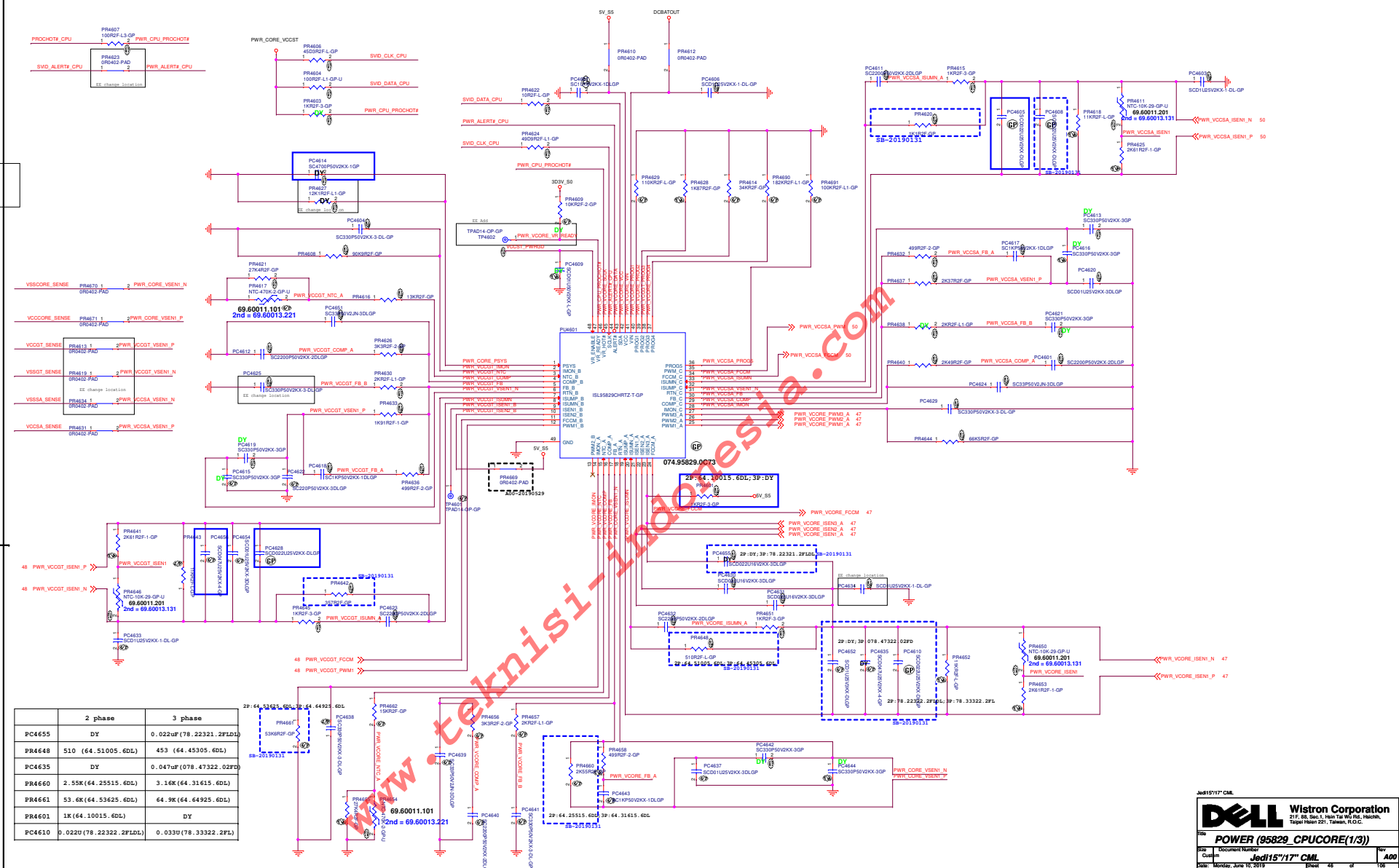
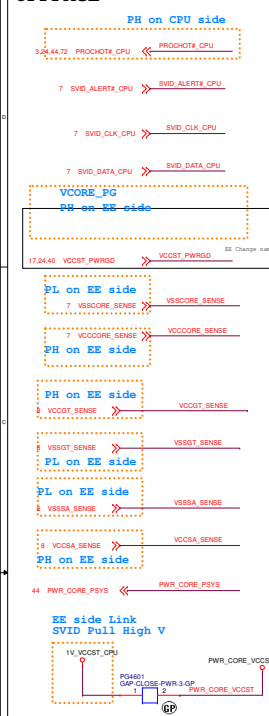


MIN	TYP	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Automatic charging	DEFAULT ACINRES
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
22.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
62.9				1MHz	No	0.476
75.5				1MHz	No	1.5
92.5				733kHz	No	0.476
105				733kHz	No	0.476
118			3	733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476



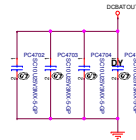
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>Power (SY8288/8286 5V/3D3V)</b>	
<b>Size</b> A2	<b>Document Number</b> <b>Jedi15"/17" CML</b>
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<b>Rev</b> <b>A00</b>	

Main FUNC = CPU CORE OFFPAGE



	2 phase	3 phase
PC4655	DY	0.022uF (78.22321.2FLD)
PR4648	510 (64.51005.6DL)	453 (64.45305.6DL)
PC4635	DY	0.047uF (078.47322.02FD)
PR4660	2.55K (64.25515.6DL)	3.16K (64.31615.6DL)
PR4661	53.6K (64.53625.6DL)	64.9K (64.64925.6DL)
PR4601	1K (64.10015.6DL)	DY
PC4610	0.022u (78.22322.2FLD)	0.033u (78.33322.2FL)

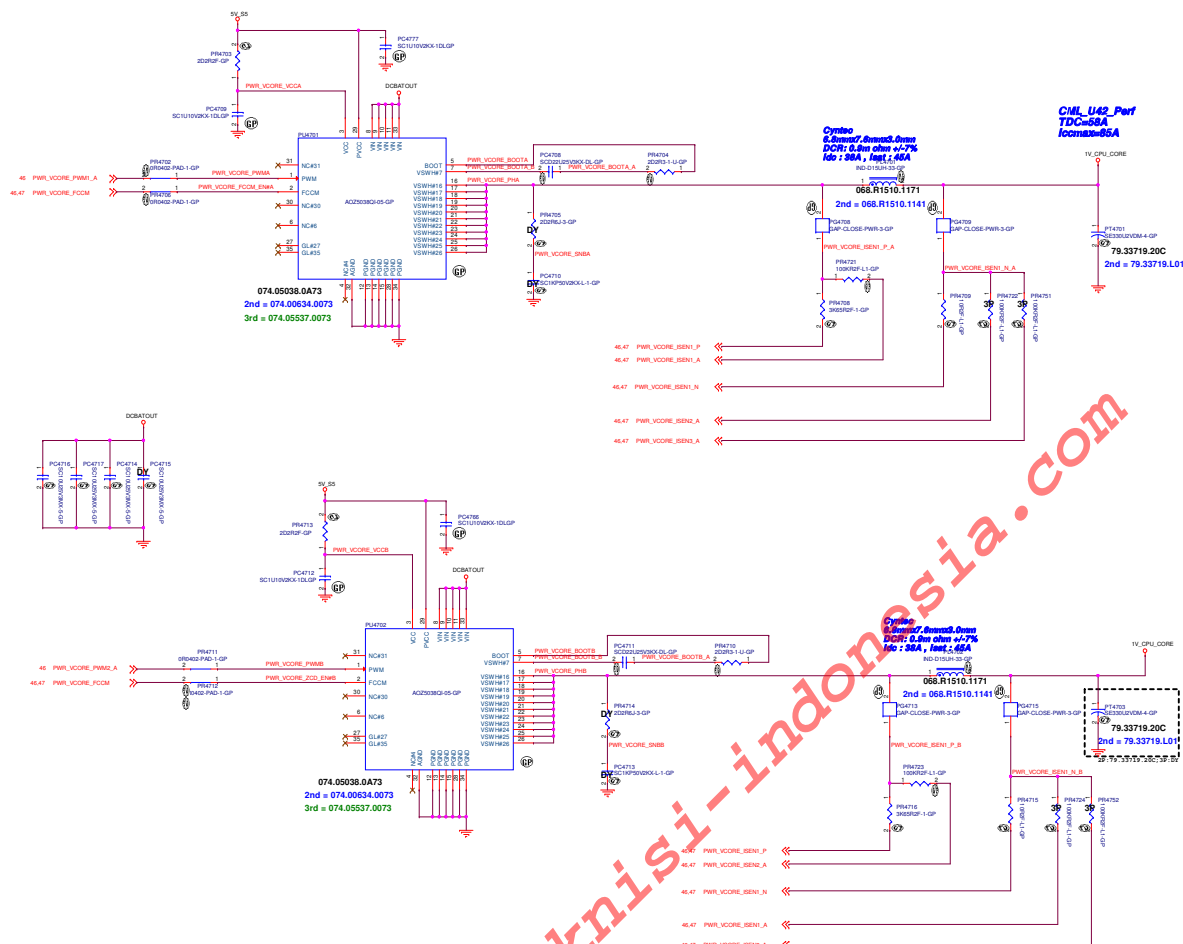
## OFFPAGE



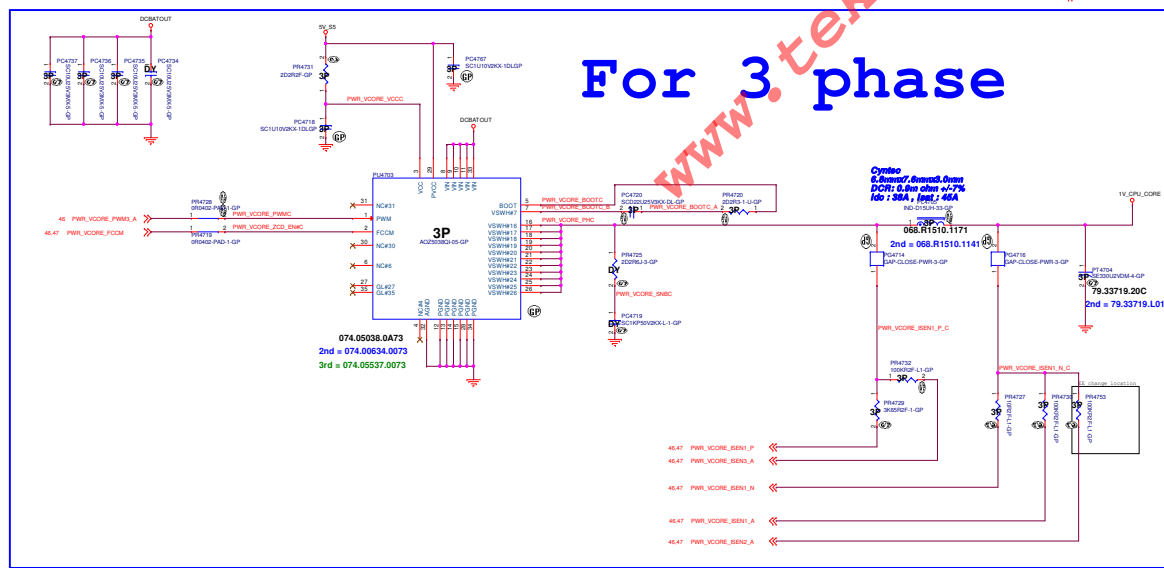
For acoustic noise



	2 phase	3 phase
PR4722	DT	100K(64.10035.6DL)
PR4751	DT	100K(64.10035.6DL)
PR4724	DT	100K(64.10035.6DL)
PR4752	DT	100K(64.10035.6DL)
PR4730	DT	100K(64.10035.6DL)
PR4753	DT	100K(64.10035.6DL)
PR4731	DT	2.2K(64.28205.6DL)
PU4703	DT	AG25038Q1-05-GP (074.05038.0A73)
PC4767	DT	1uF(78.10523.5FLDL)
PC4718	DT	1uF(78.10523.5FLDL)
PC4720	DT	0.22uF(78.22422.2MLDL)
PR4720	DT	2.2K(64.28205.55L)
PL4705	DT	0.15uH(068.R1510.1171)
PR4729	DT	3.69K(64.36515.6DL)
PR4732	DT	100K(64.10035.6DL)
PR4727	DT	10K(64.10805.131)
PC4704	DT	330uF(79.33719.20C)
PC4735	DT	10uF(078.10612.058D)
PC4736	DT	10uF(078.10612.058D)
PC4737	DT	10uF(078.10612.058D)



For 3 phase



Title <b>POWER (5038_CPU_VCORE(3/3))</b>			
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Title **CPU\_VCCGTUS**

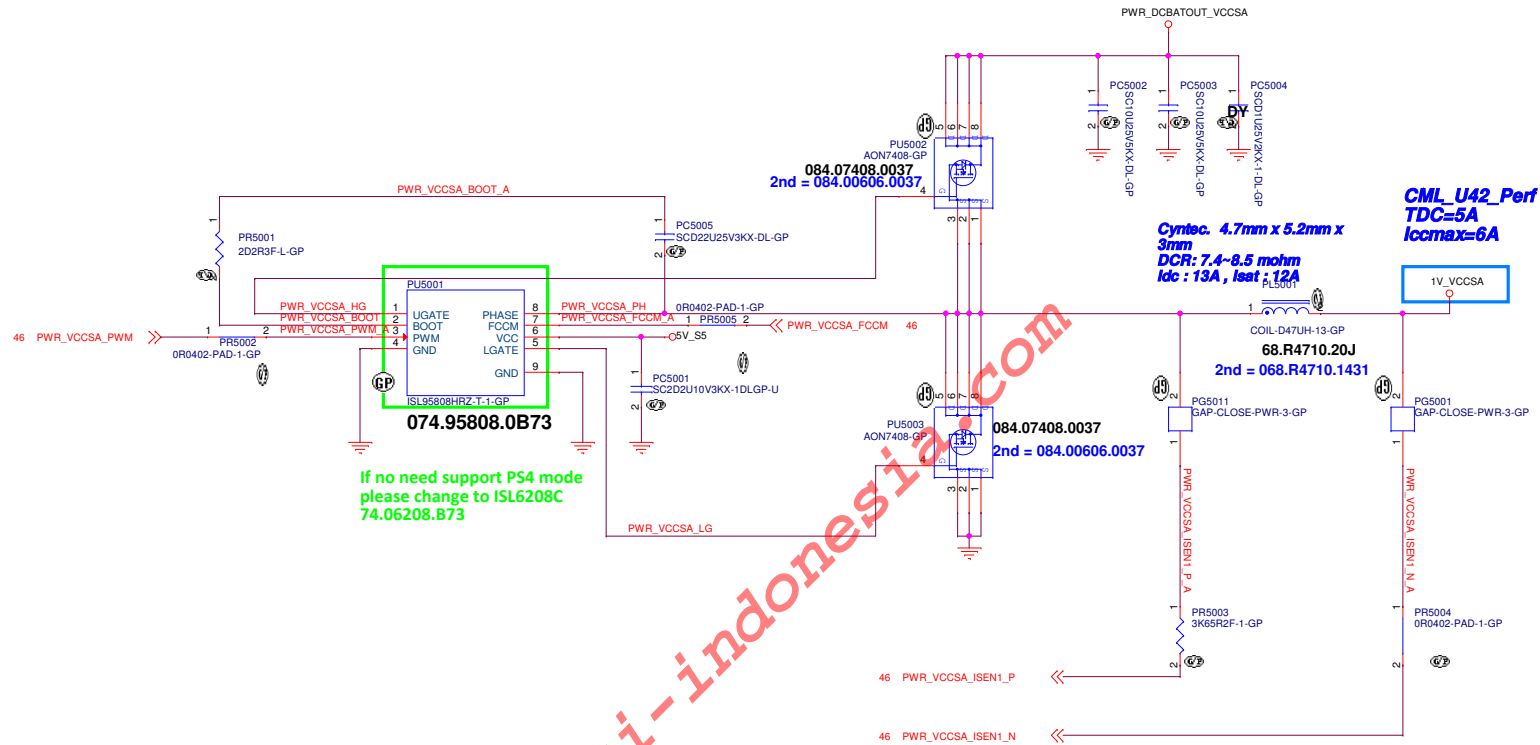
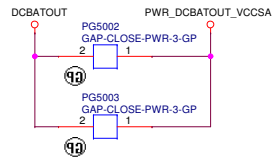
Size  
A4

Document Number  
**Jedi15"/17" CML**

Rev  
**A00**

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<b>DELL</b>		<b>Wistron Corporation</b>	
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Title <b>VCCSA</b>			
Size Custom	Document Number <b>Jedi15"/17" CML</b>		Rev <b>A00</b>
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Main Func = PWR.Plane.Regulator\_1D0V

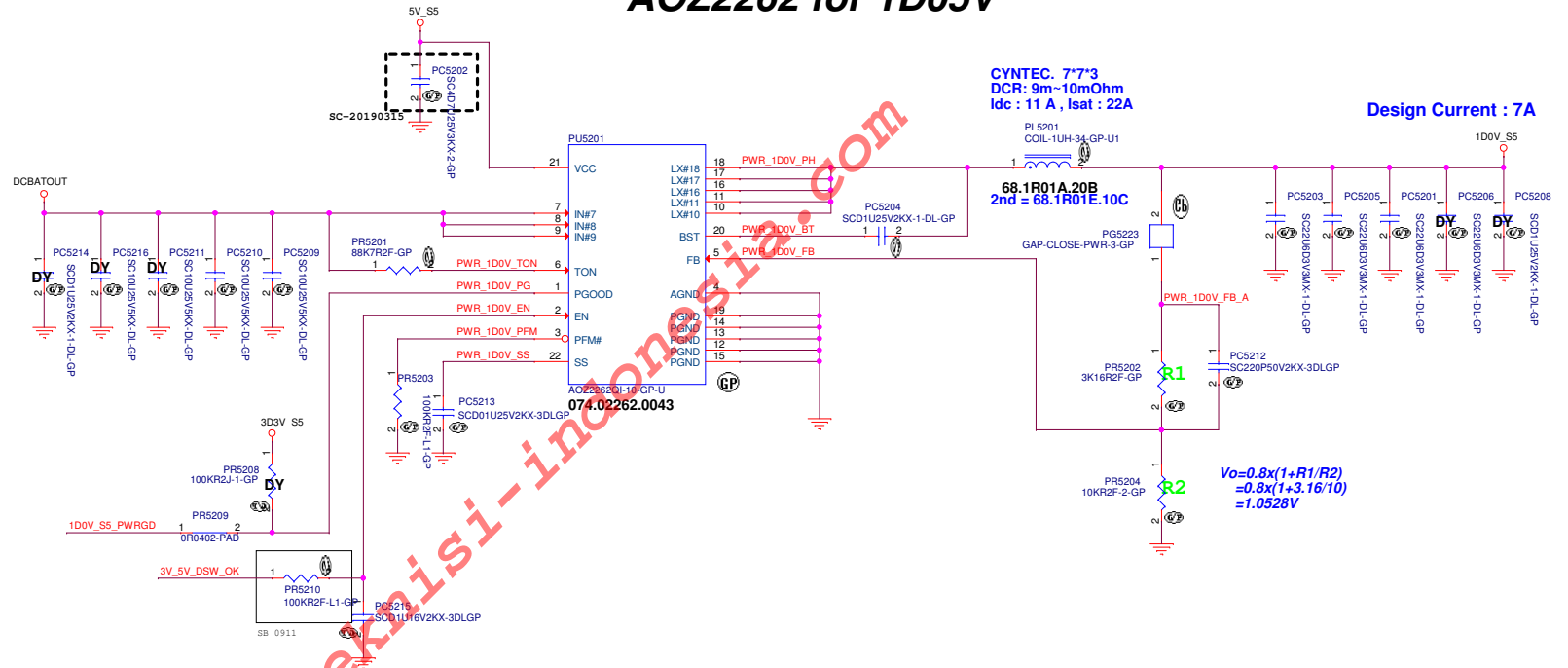
OFFPAGE-Signal

OFFPAGE-GAP

40 1D0V\_SS\_PWRGD <<<

25.53 3V\_5V\_DSW\_OK >>>

## AOZ2262 for 1D05V



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Title			(Reserved)
Size	Document Number	Rev	A00
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Main Func = 1D8V

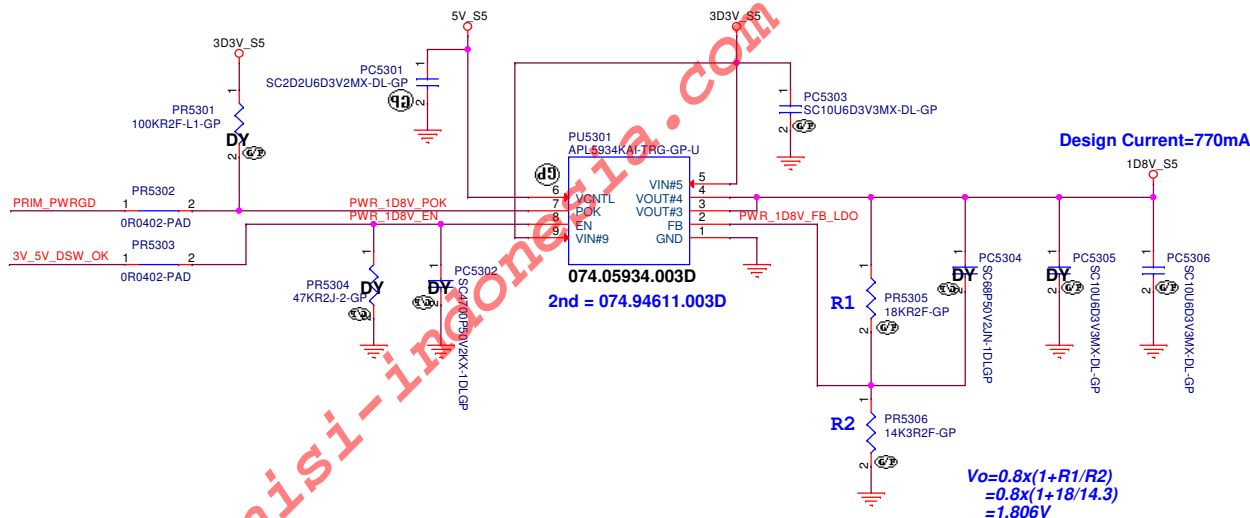
OFFPAGE-Signal

OFFPAGE-GAP

24,40 PRIM\_PWRGD <<<—

25,52 3V\_5V\_DSW\_OK >>>—

## APL5934 for 1D8V\_S5



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Main Func = 2D5V/ 1D8V

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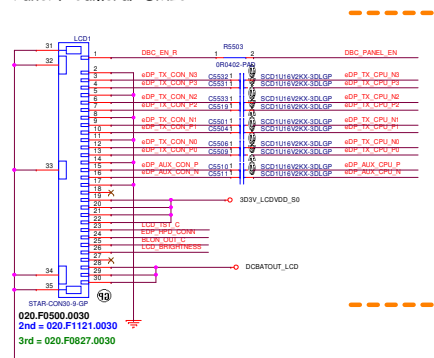
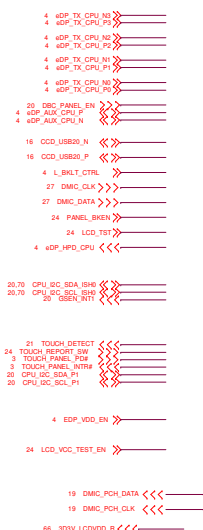
Title

(Reserved)

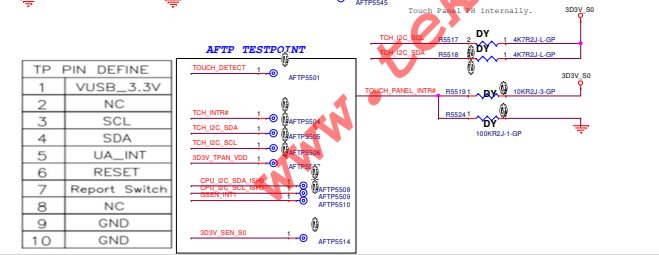
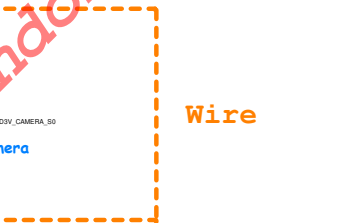
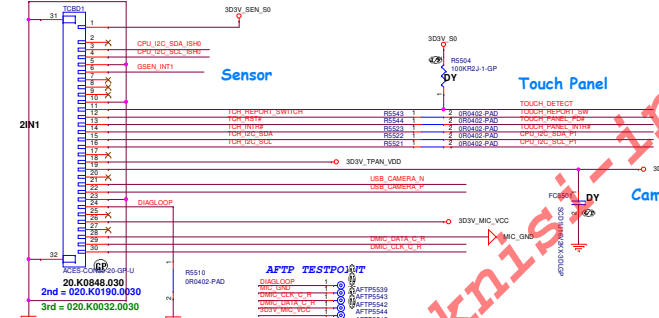
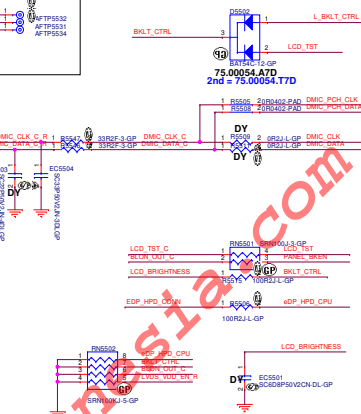
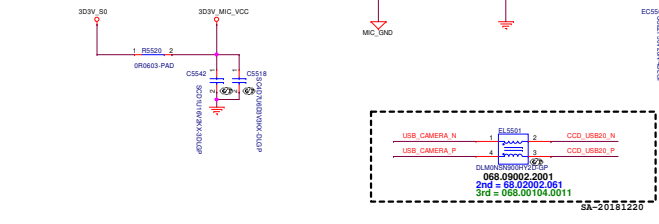
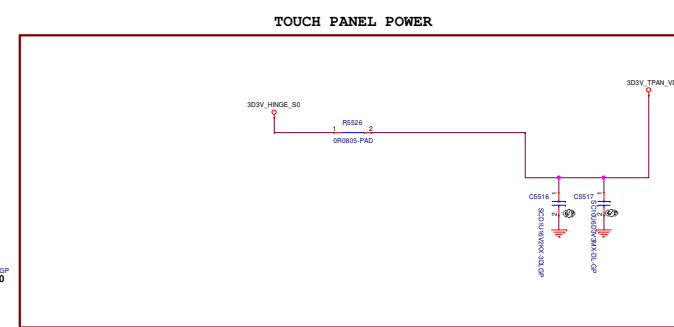
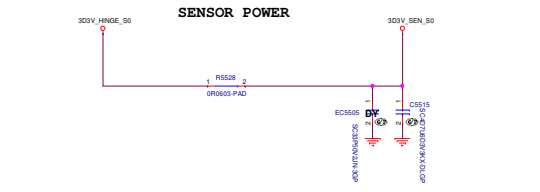
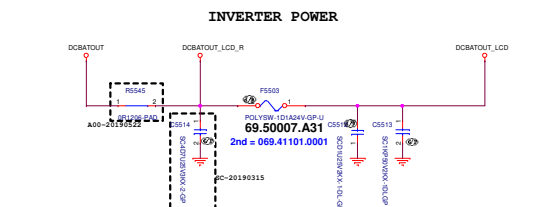
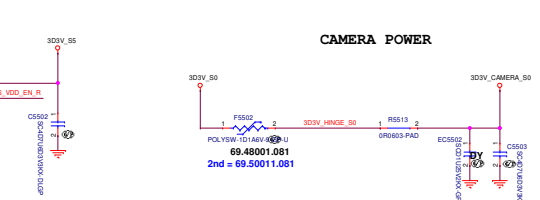
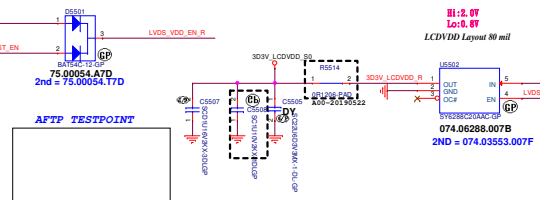
Size	Document Number	Rev
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## Panel / Camera/ DMIC



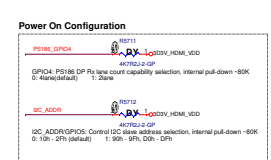
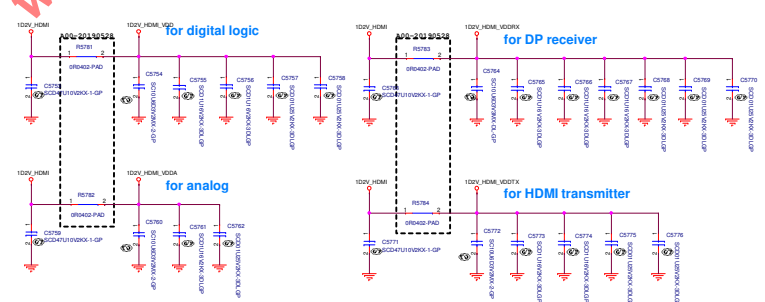
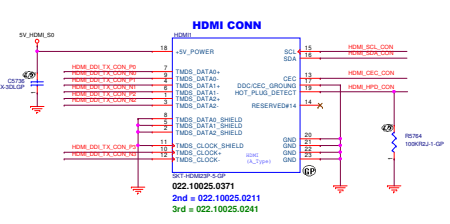
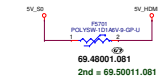
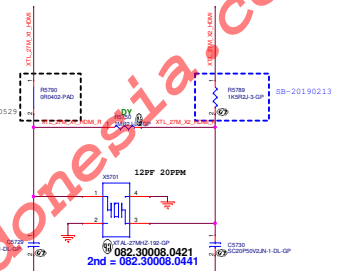
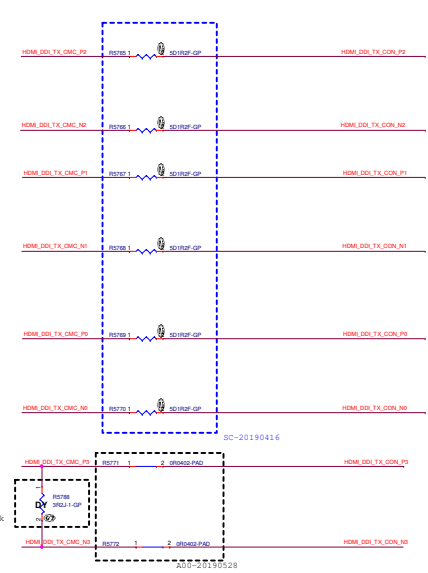
## ! Coaxial



TP	PIN	DEFINE
1		VUSB_3.3V
2		NC
3		SCL
4		SDA
5		UA_INT
6		RESET
7		Report Switch
8		NC
9		GND
10		GND

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Jedi15"/17" CML




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Title		<b>Display (RSVD) DP</b>	
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Title

Display (RSVD) DVI

Size

A3

Document Number

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Rev

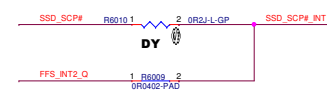
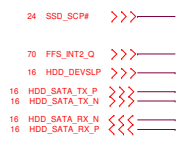
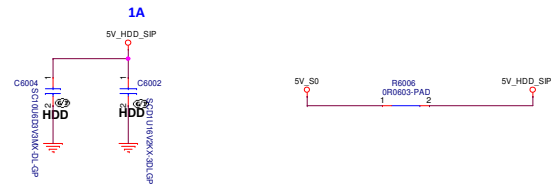
X01

Sheet

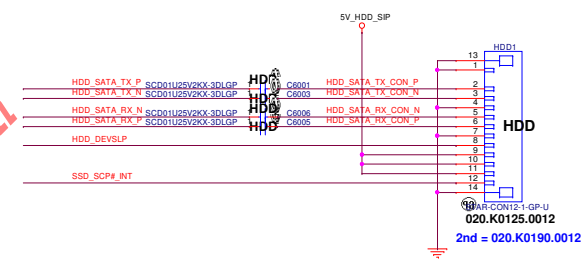
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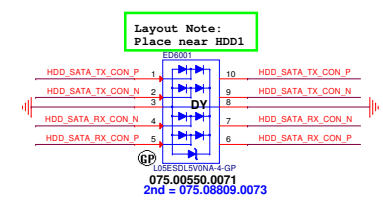
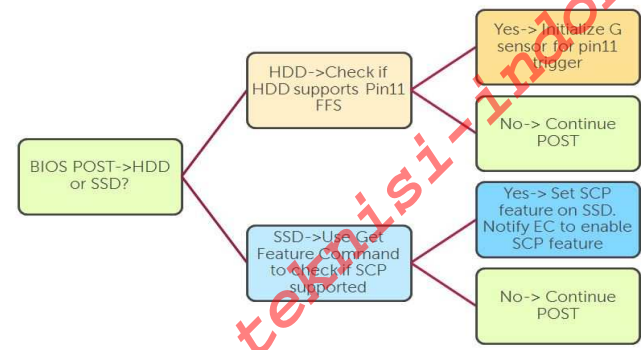
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### SATA HDD Connector



- BIOS today already check whether the device is HDD and whether it supports FFS before enabling sensor chip to trigger pin11. The plan is to add a check on the SSD path to decide if device supports SCP and notify EC whether to support SCP.






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Jedi15"/17" CML

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>INT IO (RSVD) WWAN</b>			
Size A4	Document Number <b>Jedi15"/17" CML</b>		Rev <b>X01</b>
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18 SSD\_CLKREQ\_CPU\_N <<<—  
17,26,61,66,71,76,91 PLTRST#\_CPU >>>—  
  
16 SSD\_DEVS\_LP >>>—  
18 SSD\_CLK\_CPU\_P >>>—  
16 SSD\_CLK\_CPU\_N >>>—  
16 SSD\_SATA\_TX\_P >>>—  
16 SSD\_SATA\_TX\_N >>>—  
16 SSD\_SATA\_RX\_P >>>—  
16 SSD\_SATA\_RX\_N >>>—  
16 SSD\_PCIE\_TX\_P3 >>>—  
16 SSD\_PCIE\_RX\_P3 >>>—  
16 SSD\_PCIE\_TX\_N3 >>>—  
16 SSD\_PCIE\_RX\_N3 >>>—  
16 SSD\_PCIE\_TX\_P2 >>>—  
16 SSD\_PCIE\_RX\_P2 >>>—  
16 SSD\_PCIE\_TX\_N2 >>>—  
16 SSD\_PCIE\_RX\_N2 >>>—  
16 SSD\_PCIE\_TX\_P1 >>>—  
16 SSD\_PCIE\_RX\_P1 >>>—  
16 SSD\_PCIE\_TX\_N1 >>>—  
16 SSD\_PCIE\_RX\_N1 >>>—  
  
16 M2\_SSD\_PEDET <<<—  
64 SSD\_LED# <<<—  
  
24 SSD\_SCP#\_M2 >>>—

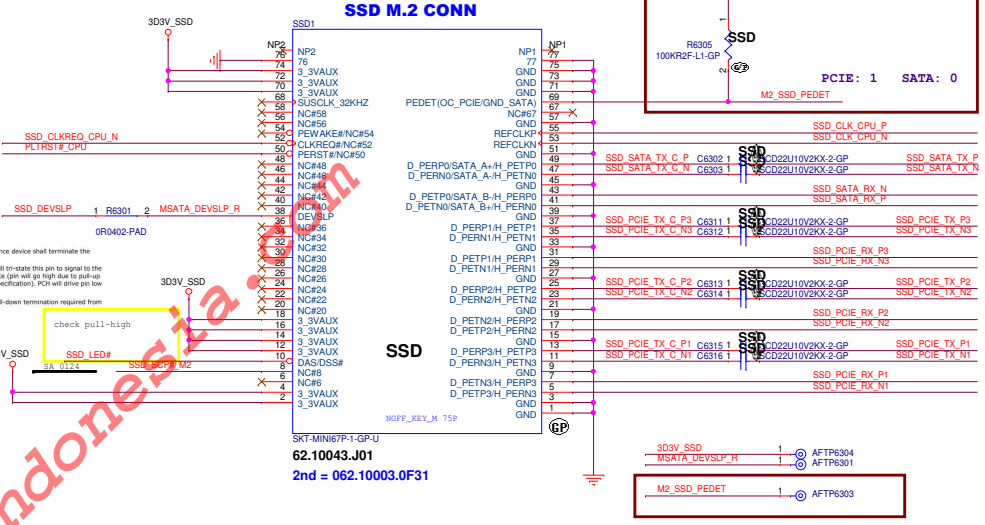
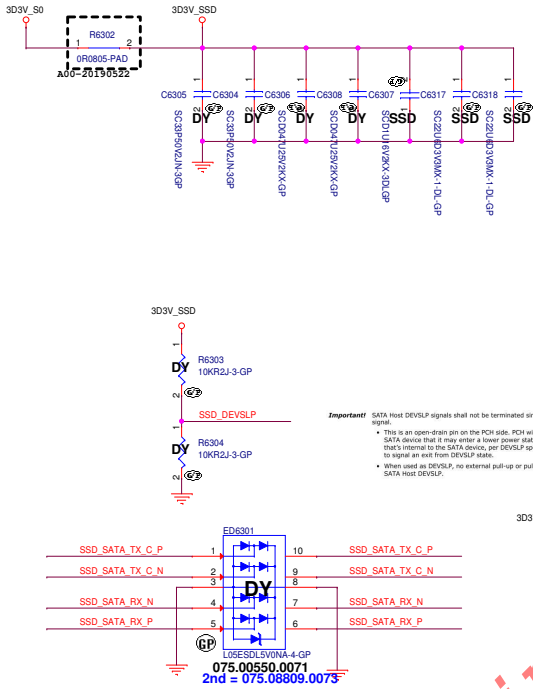


Table 13-12. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>


**Notes:**

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe\* lane that needs to support either PCIe\* Gen2 devices or PCIe\* Gen3 devices, follow the PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Pin	Signal	Pin	Signal
1	3.3V	27	NC
2	3.3V	28	NC
3	3.3V	29	NC
4	3.3V	30	NC
5	3.3V	31	NC
6	3.3V	32	NC
7	3.3V	33	NC
8	3.3V	34	NC
9	3.3V	35	NC
10	3.3V	36	NC
11	3.3V	37	NC
12	3.3V	38	NC
13	3.3V	39	NC
14	3.3V	40	NC
15	3.3V	41	NC
16	3.3V	42	NC
17	3.3V	43	NC
18	3.3V	44	NC
19	3.3V	45	NC
20	3.3V	46	NC
21	3.3V	47	NC
22	3.3V	48	NC
23	3.3V	49	NC
24	3.3V	50	NC
25	3.3V	51	NC
26	3.3V	52	NC
27	3.3V	53	NC
28	3.3V	54	NC
29	3.3V	55	NC
30	3.3V	56	NC
31	3.3V	57	NC
32	3.3V	58	NC
33	3.3V	59	NC
34	3.3V	60	NC
35	3.3V	61	NC
36	3.3V	62	NC
37	3.3V	63	NC
38	3.3V	64	NC
39	3.3V	65	NC
40	3.3V	66	NC
41	3.3V	67	NC
42	3.3V	68	NC
43	3.3V	69	NC
44	3.3V	70	NC
45	3.3V	71	NC
46	3.3V	72	NC
47	3.3V	73	NC
48	3.3V	74	NC
49	3.3V	75	NC
50	3.3V	76	NC
51	3.3V	77	NC
52	3.3V	78	NC
53	3.3V	79	NC
54	3.3V	80	NC
55	3.3V	81	NC
56	3.3V	82	NC
57	3.3V	83	NC
58	3.3V	84	NC
59	3.3V	85	NC
60	3.3V	86	NC
61	3.3V	87	NC
62	3.3V	88	NC
63	3.3V	89	NC
64	3.3V	90	NC
65	3.3V	91	NC
66	3.3V	92	NC
67	3.3V	93	NC
68	3.3V	94	NC
69	3.3V	95	NC
70	3.3V	96	NC
71	3.3V	97	NC
72	3.3V	98	NC
73	3.3V	99	NC
74	3.3V	100	NC

Jedi15/17 CML



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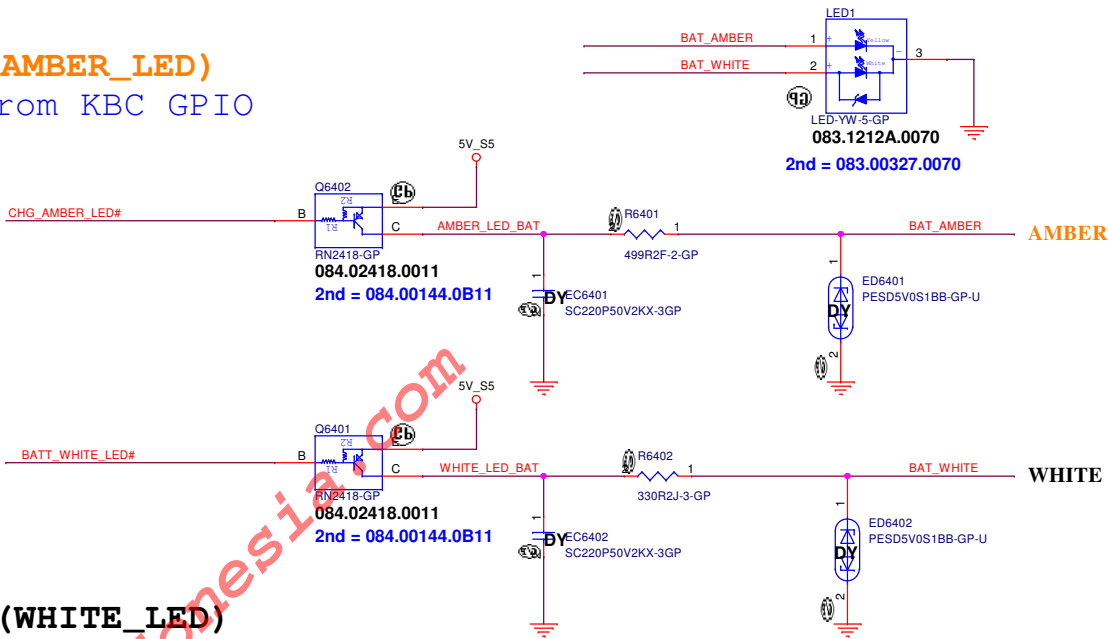
Title: **INT IO (SSD M.2/ eMMC)**

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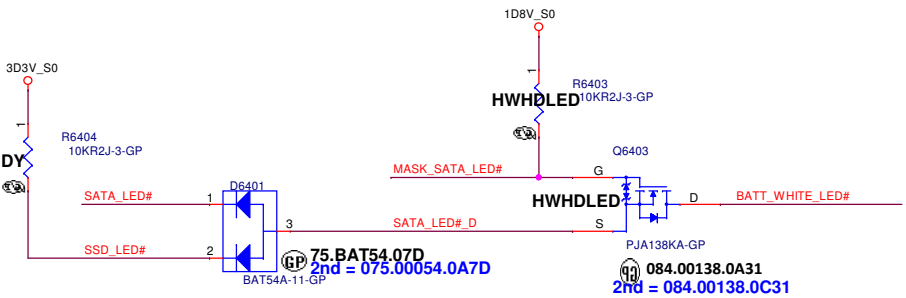
24.90 CHG\_AMBER\_LED# >>>—  
24 BATT\_WHITE\_LED# >>>—

Battery LED1 (AMBER\_LED)  
Low activated from KBC GPIO



Battery LED2 (WHITE\_LED)  
Low activated from KBC GPIO

16 SATA\_LED# >>>—  
63 SSD\_LED# >>>—  
24 MASK\_SATA\_LED# >>>—



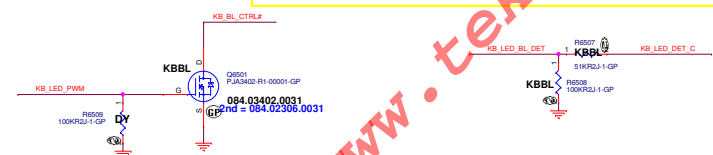
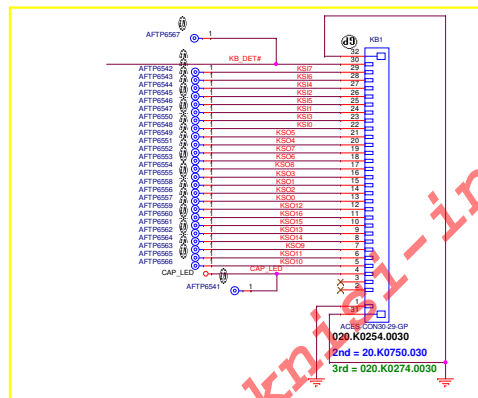
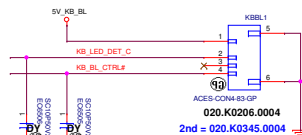
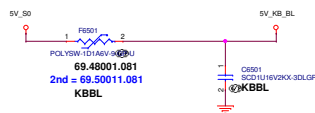


## Main Func = Keyboard

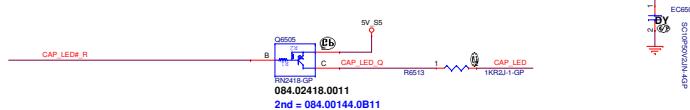
24 KSQ[0..7] >>> \_\_\_\_\_  
 24 KSQ[8..16] <<< \_\_\_\_\_

24 PTP\_DIS# >>> \_\_\_\_\_  
 3,24 TP\_WAKE\_KBC# <<< \_\_\_\_\_  
 24 CLK\_TP\_SIO <<< \_\_\_\_\_  
 24 DAT\_TP\_SIO <<< \_\_\_\_\_  
 20,66 CPU\_BC\_SCL\_P0 >>> \_\_\_\_\_  
 20,66 CPU\_BC\_SDA\_P0 >>> \_\_\_\_\_  
 19 KB\_LED\_BL\_DET <<< \_\_\_\_\_  
 20 KB\_DET# <<< \_\_\_\_\_  
 24 KB\_LED\_PWM >>> \_\_\_\_\_  
 24 CAP\_LED#\_R >>> \_\_\_\_\_

KB Backlight Power Consumption: 285mA max.



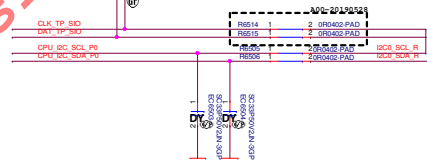
**CAP LED Control**  
 LOW acted from KBC GPIO



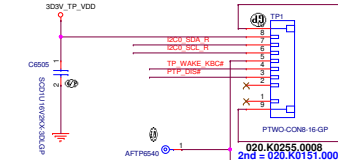
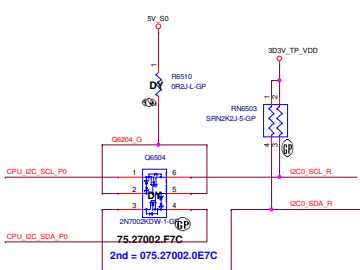
## Main Func = TPAD



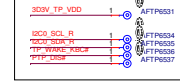
EC I2C  
 CPU I2C



Need to check if it is Active High or Active Low  
 and check if there is a pull-up on TPA side.



**AFTP TESTPOINT**

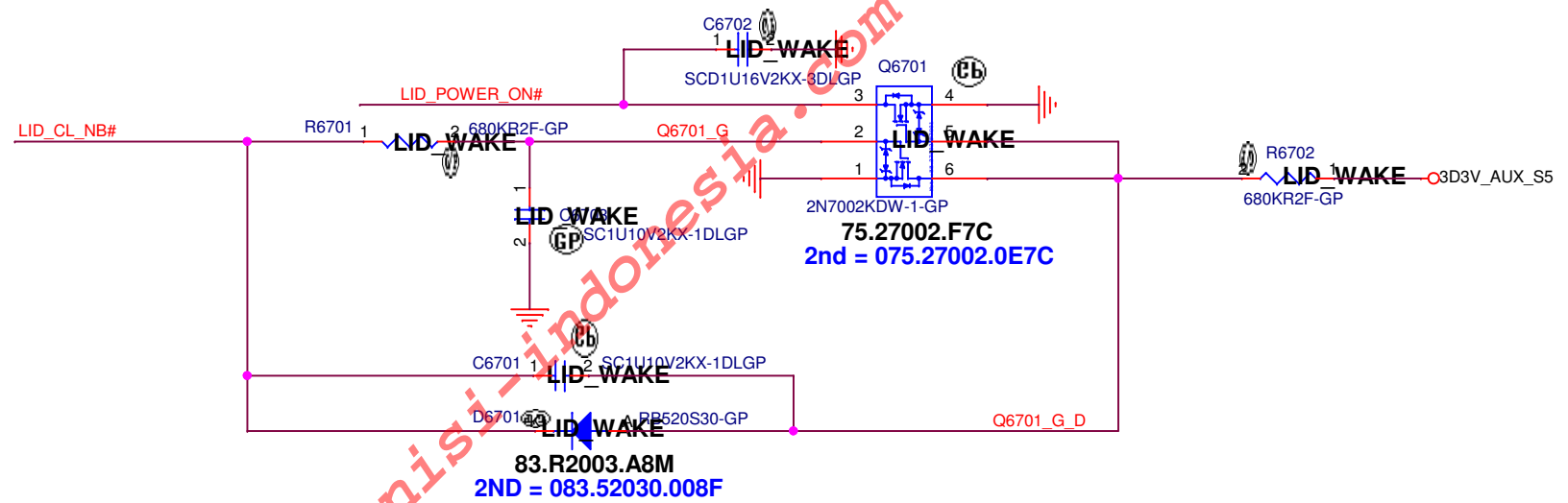


Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



# Main Func = HALL SENSOR

69 LID\_CL\_NB# >>>  
24 LID\_POWER\_ON# <<<



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**Lid\_Wake**

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A4

Document Number

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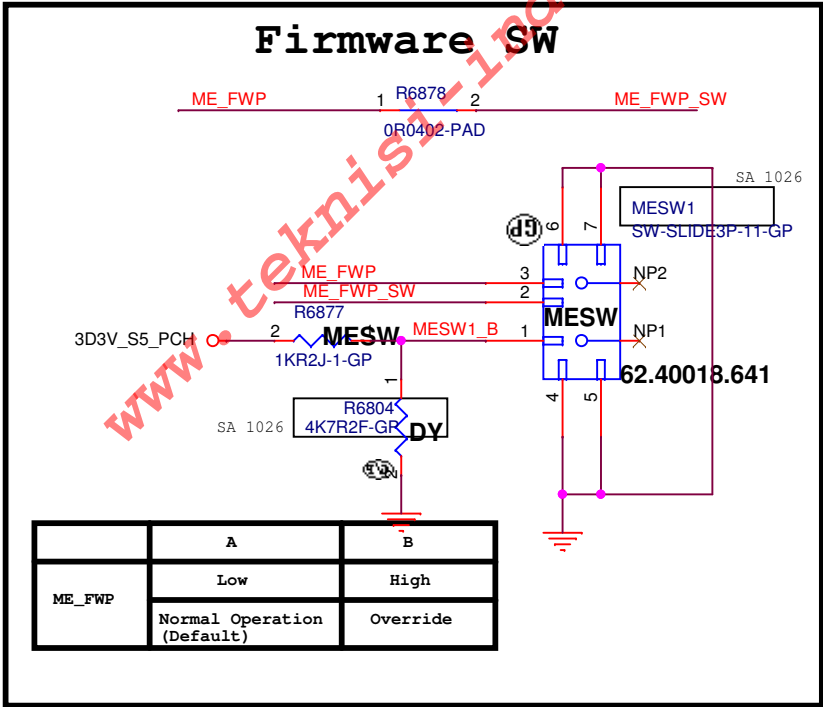
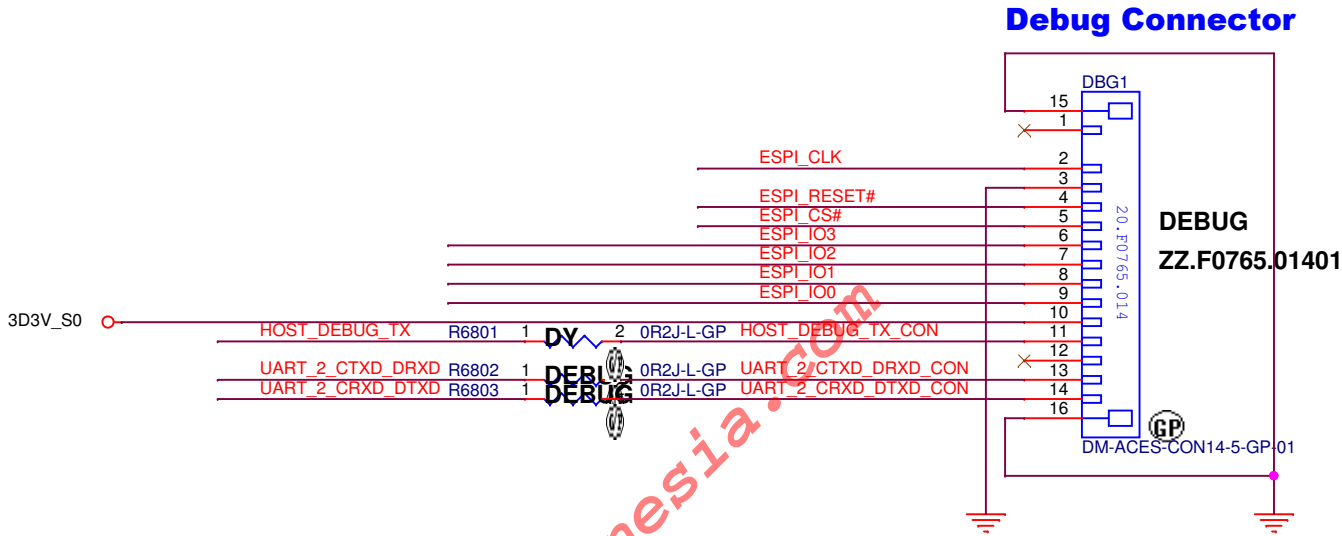
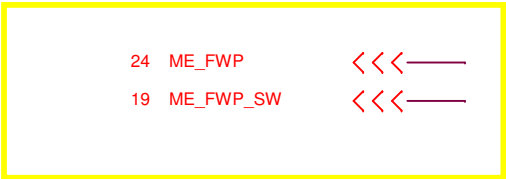
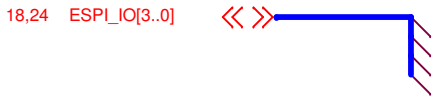
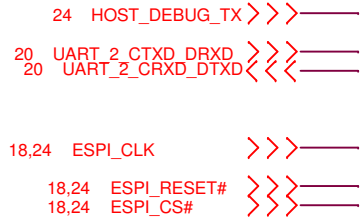
Rev

**A00**


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Main Func = Debug



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**Debug (LPC debug)**

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**X01**

Date: Monday, June 10, 2019

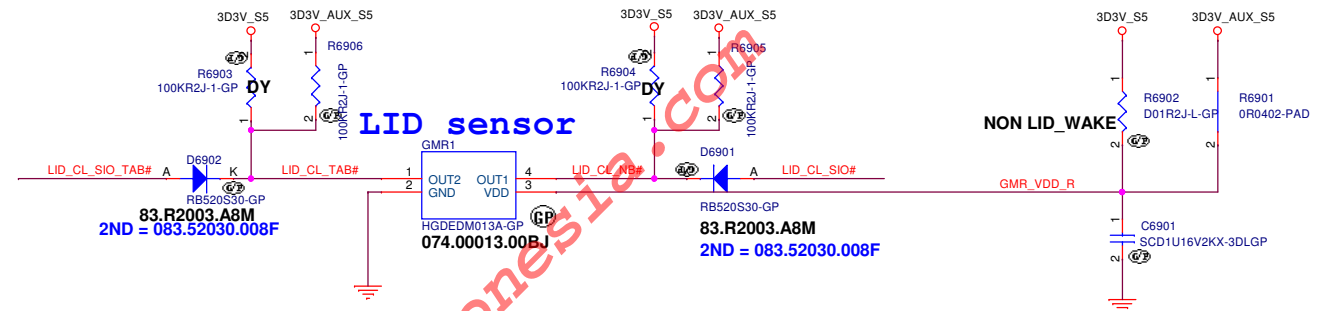
Sheet 68 of 106

5  
Main FUNC = GMR

20,24,66 LID\_CL\_SIO# >>>\_\_\_\_\_

20,24,66 LID\_CL\_SIO\_TAB#&lt;&lt;&lt;\_\_\_\_\_

67 LID\_CL\_NB# &lt;&lt;&lt;\_\_\_\_\_



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### Sensor (RSVD)

Size  
A3

Document Number
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**Jedi15"/17" CML**

Rev	<b>X01</b>
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Date: Monday, June 10, 2019

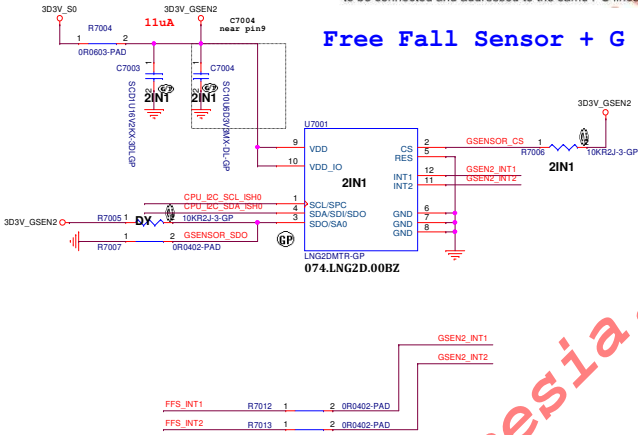
Sheet	69	of	106
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Main Func = Free Fall Sensor

20.55 CPU\_IC\_SCL\_ISH0 <<<<  
20.55 CPU\_IC\_SDA\_ISH0 <<<<  
20 GSEN2\_INT1 <<<<  
  
18 FFS\_INT1 <<<<  
  
20 FFS\_INT2 <<<<  
60 FFS\_INT2\_Q <<<<

The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I<sup>2</sup>C lines.

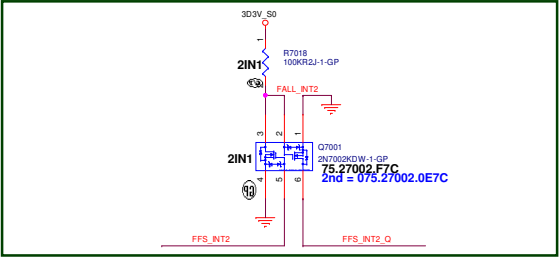
Free Fall Sensor + G Sensor



**Note:**

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U7001

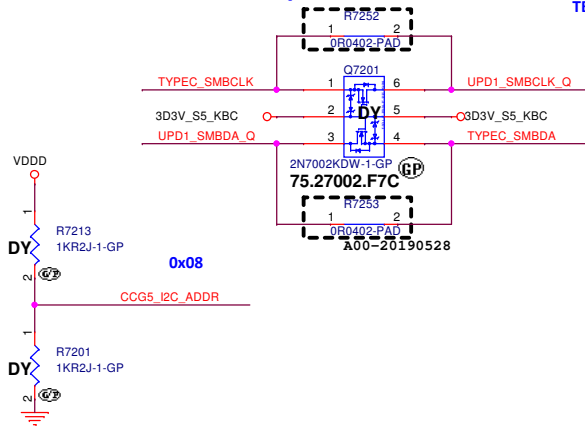
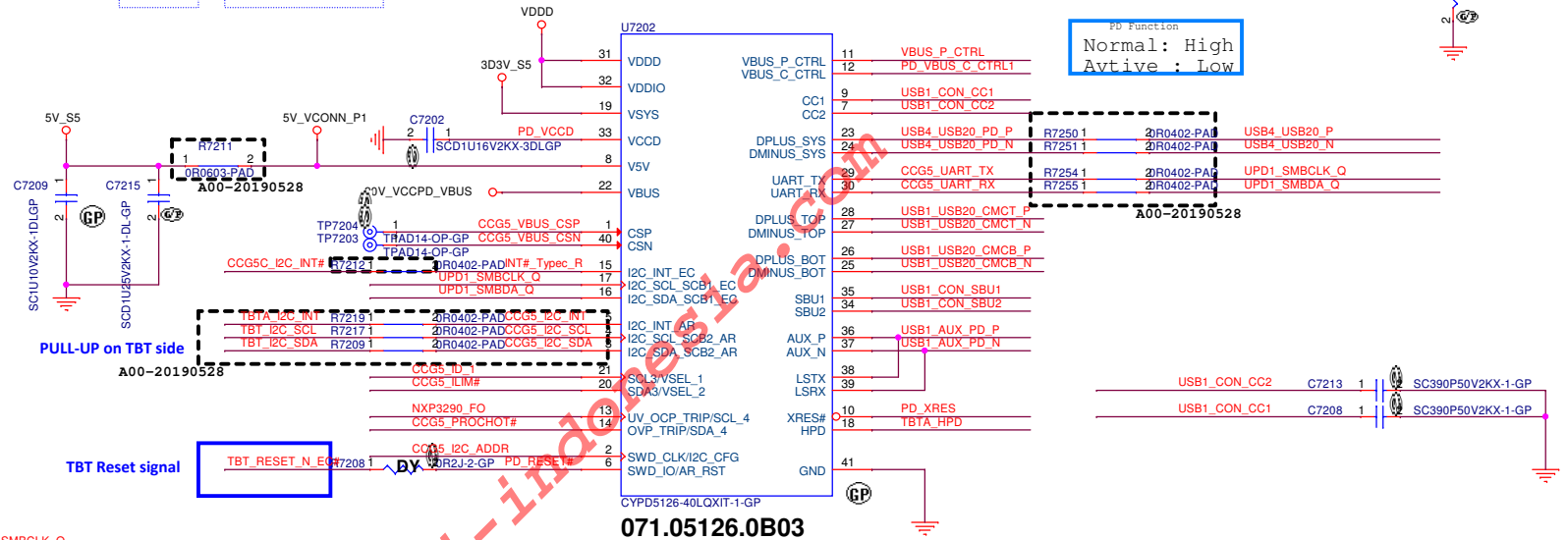
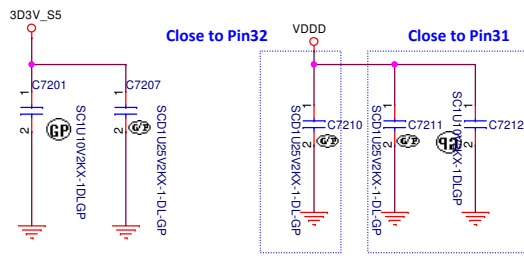
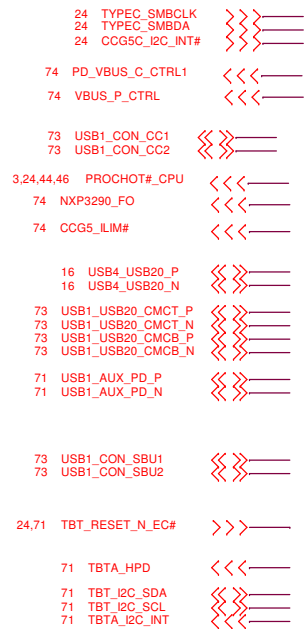


**Note:**

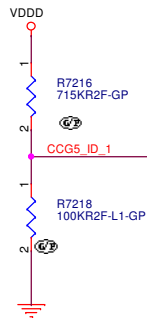
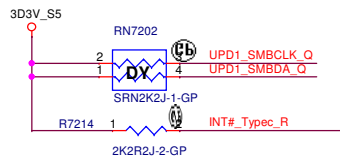
(1) Keep all signals are the same trace width. (included VDD, GND).  
(2) No VIA under IC bottom.



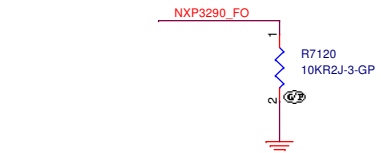
## Main Func = TypeC



COG5's I2C address is decided by the SMD clock pin.  
Don't mount R8 and R9 for the I2C address 0x08. This is the default one.  
Mount only R9 for the I2C address 0x40.  
Mount only R8 for the I2C address 0x42.



	Mux MOD_ID Settings			Voltage Levels <sup>1</sup>
MUX	MOD_ID1	MOD_ID2	Description	
Titan Ridge	L1	N/A	TBT Configuration	L0 = 0V <sup>2</sup>
PS8802	L4	L0	PS8802 Equalizer config #1	L1 = VDD0/8 <sup>3</sup>
PS8802	L4	L1 - L3	Reserved for PS8802 Equalizer config #2,3,4 reserved	L2 = 2*VDD0/8 <sup>3</sup>
ANX7443	L5	L0	ANX7443 Equalizer config #1	L3 = 3*VDD0/8 <sup>3</sup>
ANX7443	L5	L1 - L3	Reserved for ANX7443 Equalizer config #2,3,4 reserved	L4 = 4*VDD0/8 <sup>3</sup>
TUSB546	L6	L0	TUSB546 Equalizer config #1	L5 = 5*VDD0/8 <sup>3</sup>
TUSB546	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved	L6 = 6*VDD0/8 <sup>3</sup>
TUSB544	L6	L4	TUSB544 Equalizer config #1	L7 = 7*VDD0/8 <sup>3</sup>
TUSB544	L6	L5 - L7	Reserved for TUSB544 Equalizer config #2,3,4 reserved	



**For Debug**



**Jedi15"/17" CML**



**EXT IO (Thunderbolt(2/3)/Type C CC Logic)**

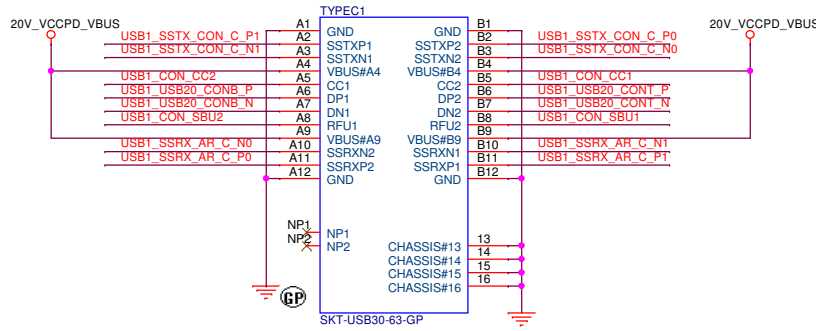
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# Main Func = TypeC

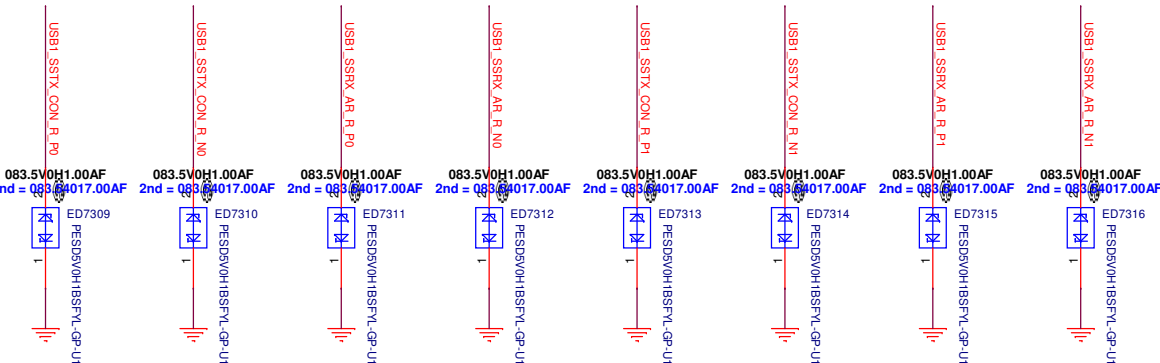
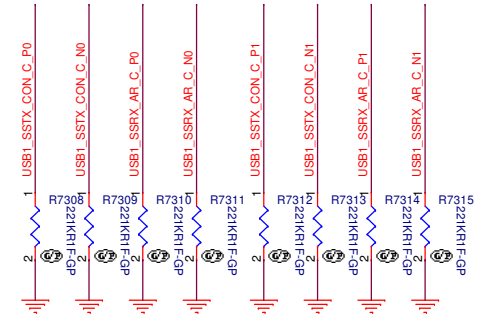
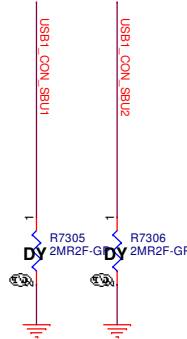
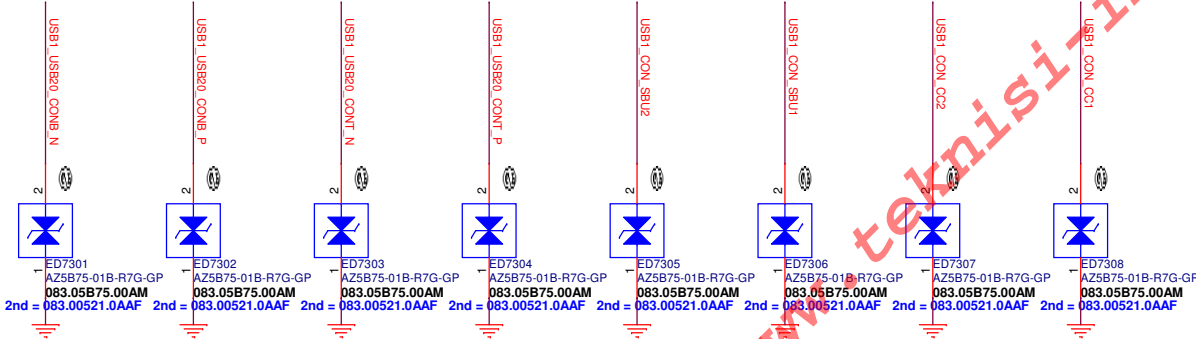
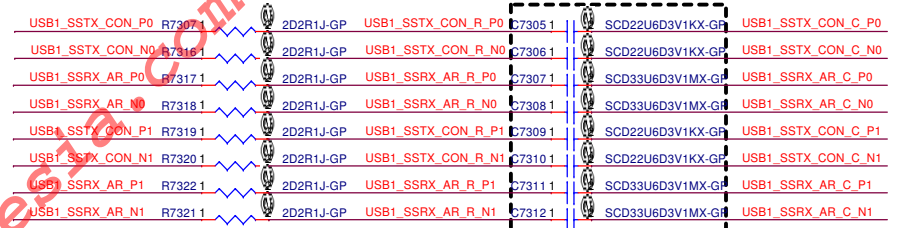
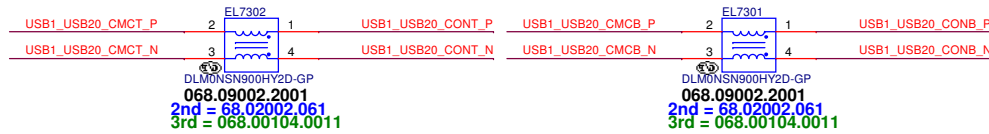
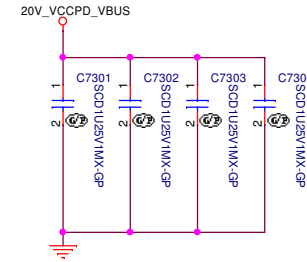
## USB1

71 USB1\_SSTX\_CON\_P0  
71 USB1\_SSTX\_CON\_N0  
71 USB1\_SSTX\_CON\_P1  
71 USB1\_SSTX\_CON\_N1  
71 USB1\_SSRX\_AR\_P0  
71 USB1\_SSRX\_AR\_N0  
71 USB1\_SSRX\_AR\_P1  
71 USB1\_SSRX\_AR\_N1  
  
72 USB1\_USB20\_CMCT\_P  
72 USB1\_USB20\_CMCT\_N  
72 USB1\_USB20\_CMCB\_P  
72 USB1\_USB20\_CMCB\_N  
  
72 USB1\_CON\_CC1  
72 USB1\_CON\_CC2  
  
72 USB1\_CON\_SBU1  
72 USB1\_CON\_SBU2



062.10009.M028

2nd = 062.10009.M039 SB-20190117



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Title  
**EXT IO (Thunderbolt(3)/Type C Conn)**

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# Main FUNC = LPS

72 PD\_VBUS\_C\_CTRL1 >>>  
72 VBUS\_P\_CTRL >>>  
72 CCG5\_ILIM# >>>  
44 VCCPD\_VBUS\_ACK >>>  
72 NXP3290\_FO >>>  
24 TYPEC\_DCIN1\_EN# >>>

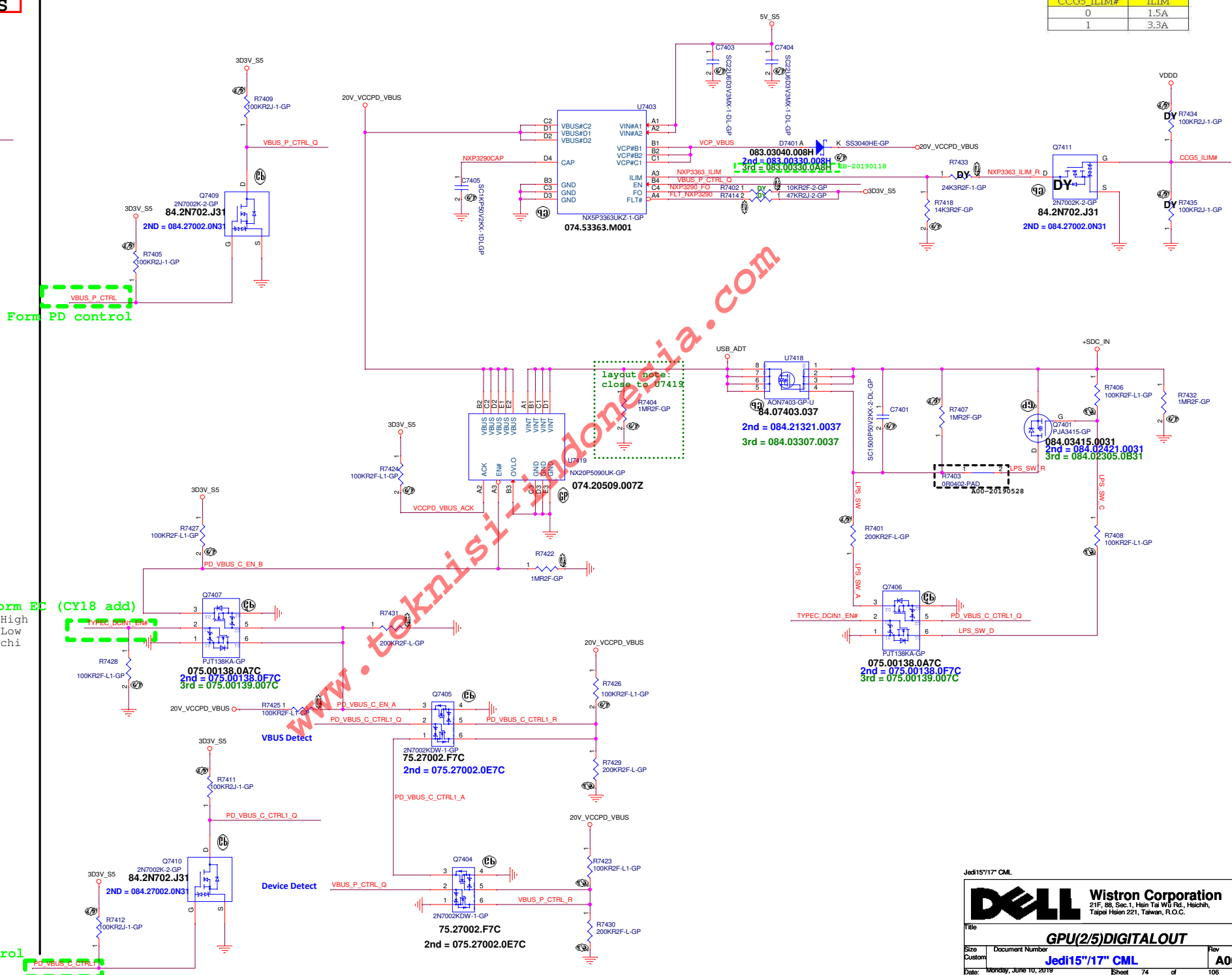
Form PD control

Form EC (CY18 add)  
Default: High  
Active : Low  
R013 Shauchi

Form PD control

Form PD control

CCG5_ILIM#	ILIM
0	1.5A
1	3.3A



Jed15717 CML

<b>DELL</b>		<b>Wistron Corporation</b>	
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File <b>GPU(2/5)DIGITALOUT</b>			
Size	Document Number	Rev	
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Title

***EXT IO (TYPEC Redriver/MUX)***

Size  
A

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Rev

***A00***

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- 79 SYS\_RST\_MOM >>>
- 18 GFX\_CLK\_CPU\_P >>>
- 18 GFX\_CLK\_CPU\_N >>>
- 26 DGPU\_HOLD\_RSTN >>>
- 17.26.61.80.66.71.81 PLTRSTN\_CPU >>>
- 85 VSACORE\_VDD\_SENSE\_1 <<<
- 85 VSACORE\_GND\_SENSE\_1 <<<
- 18 CLK\_PCIE\_PEG\_REQ <<<
- 18 GFX\_PCIE\_RX\_P0 <<<
- 18 GFX\_PCIE\_RX\_N0 <<<
- 18 GFX\_PCIE\_TX\_P0 <<<
- 18 GFX\_PCIE\_TX\_N0 <<<
- 18 GFX\_PCIE\_RX\_P1 <<<
- 18 GFX\_PCIE\_RX\_N1 <<<
- 18 GFX\_PCIE\_TX\_P1 <<<
- 18 GFX\_PCIE\_TX\_N1 <<<

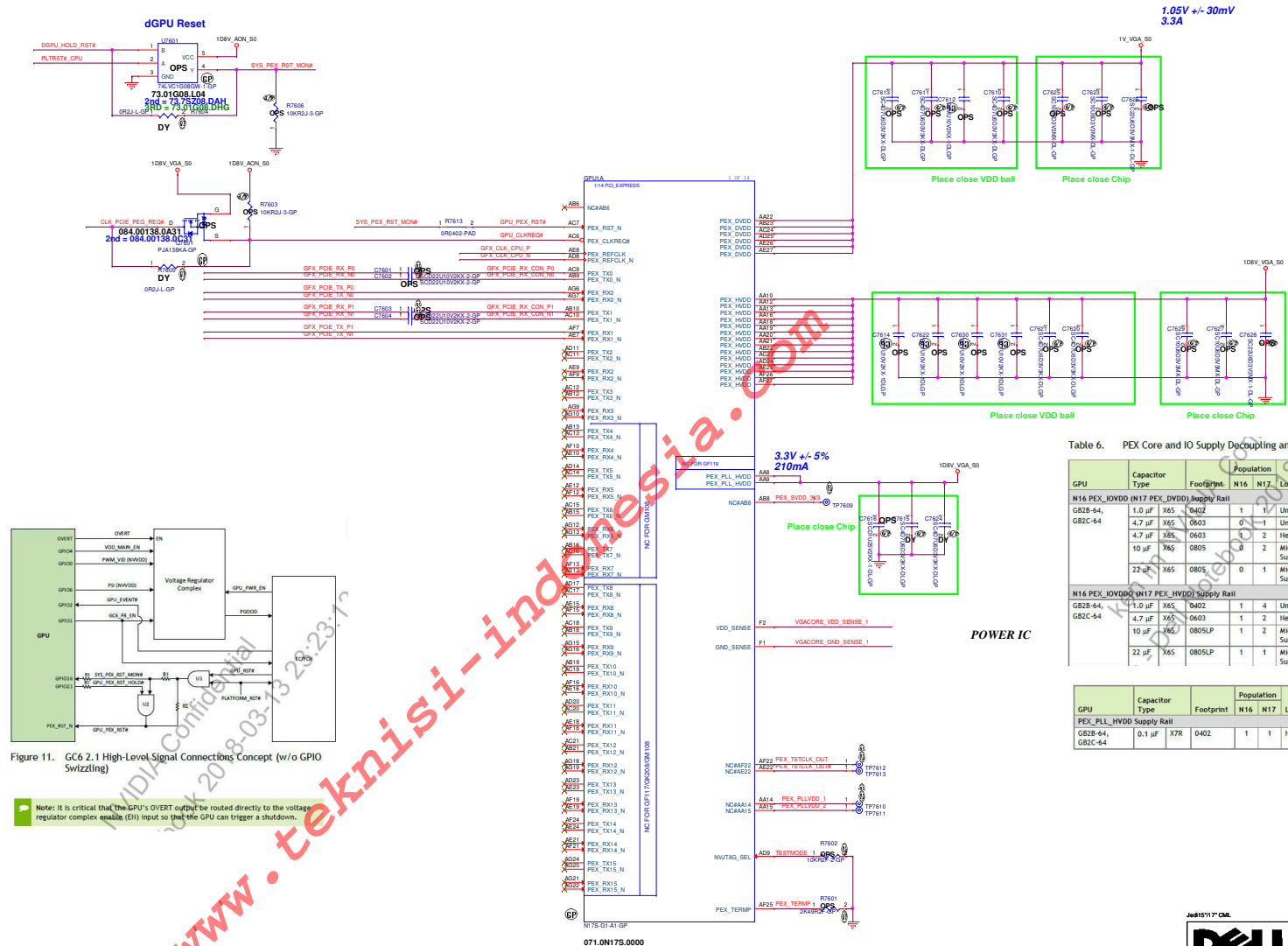


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

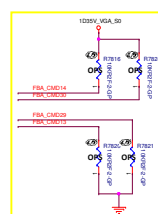
Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

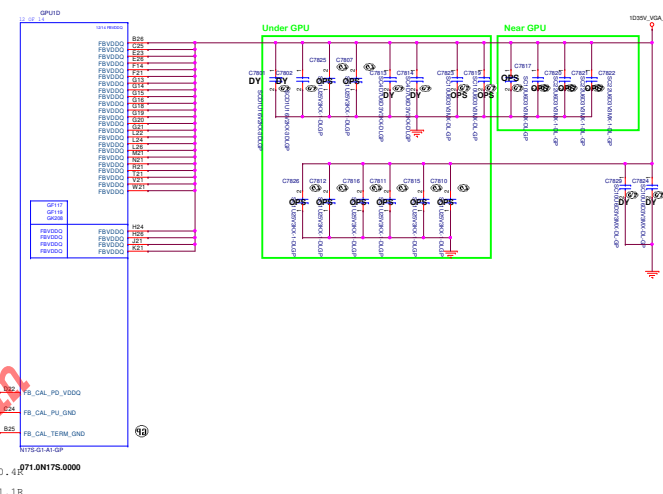
GPU	Capacitor Type	Footprint	Population	N16	N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-44, GB2C-44	1.0 uF X65	0402	1	1		Under GPU
	4.7 uF X65	0603	0	1		Under GPU
	4.7 uF X65	0603	0	2		Near GPU
	10 uF X65	0805	0	2		Midway between GPU and Power Supply
	22 uF X65	0805	0	1		Midway between GPU and Power Supply
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-44, GB2C-44	1.0 uF X65	0402	1	4		Under GPU
	4.7 uF X65	0603	1	2		Near GPU
	10 uF X65	0805LP	1	2		Midway between GPU and Power Supply
	22 uF X65	0805LP	1	1		Midway between GPU and Power Supply

GPU	Capacitor Type	Footprint	Population	N16	N17	Location
PEX_PL_LVDD Supply Rail						
GB2B-44, GB2C-44	0.1 uF	X7R	0402	1	1	Near GPU





Note:  
Reference NV-DDR5 CRB and DOH70 by GDDR5

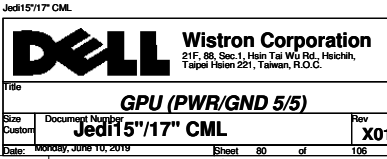


GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 $\mu$ F	X7R	0402	2	0	Under GPU
	1 $\mu$ F	X7R	0603	2	8	Under GPU
	4.7 $\mu$ F	X6S	0603	2	0	Under GPU
	10 $\mu$ F	X6S	0603	0	2	Under GPU
	10 $\mu$ F	X6S	0603	1	1	Near GPU
	22 $\mu$ F	X6S	0603W	1	3	Near GPU

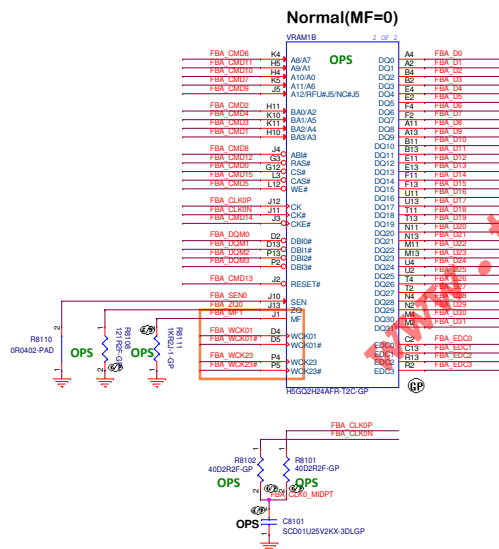
GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 $\mu$ F	X7R	0402	2	4	Under GPU
	22 $\mu$ F	X6S	0805	1	1	Near GPU
Bead Type						
	30 $\Omega$ (ESR=0.010 $\Omega$ )		0603	1	1	Near GPU



## Main Func = dGPU



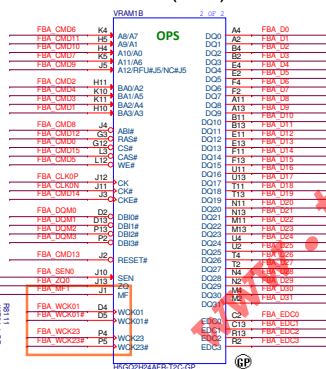


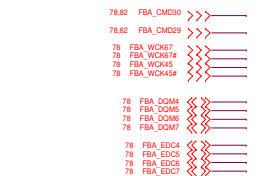
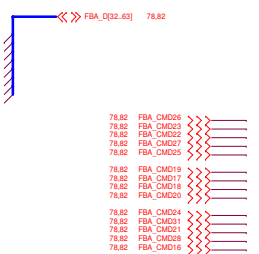
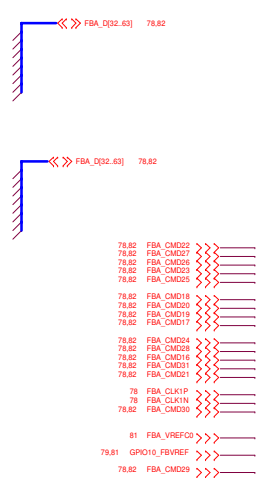


### FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPU1
Un-termination	50%	0.675V	High
Termination	70%	0.945V	Low

Normal(MF=0)

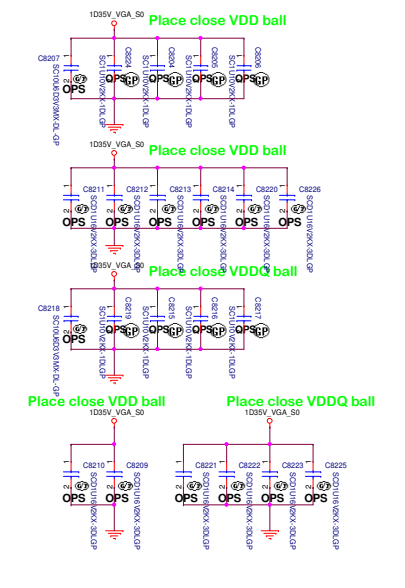
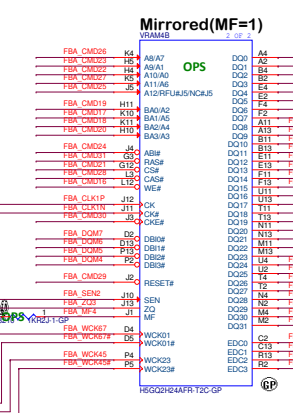
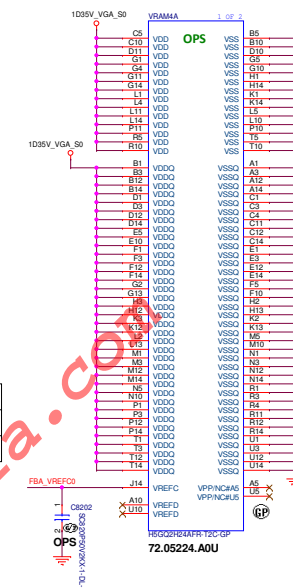




### Frame Buffer Partition A-Upper Half


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



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GPU (VRAM5,6 3/4)

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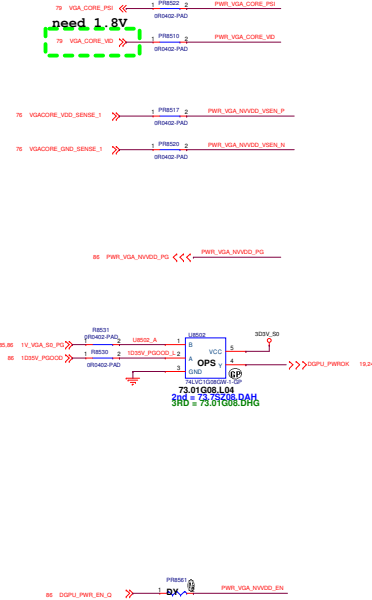
X01

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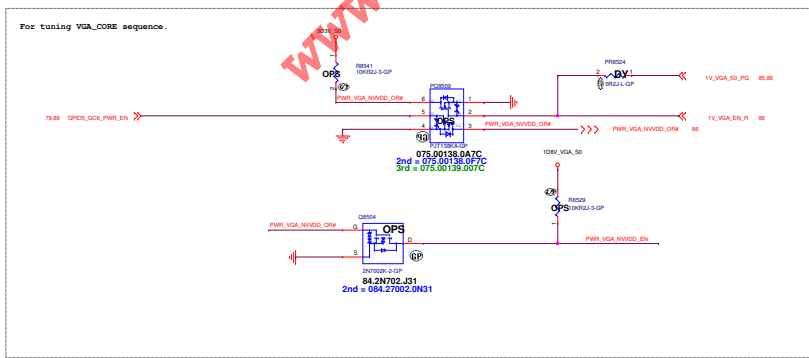
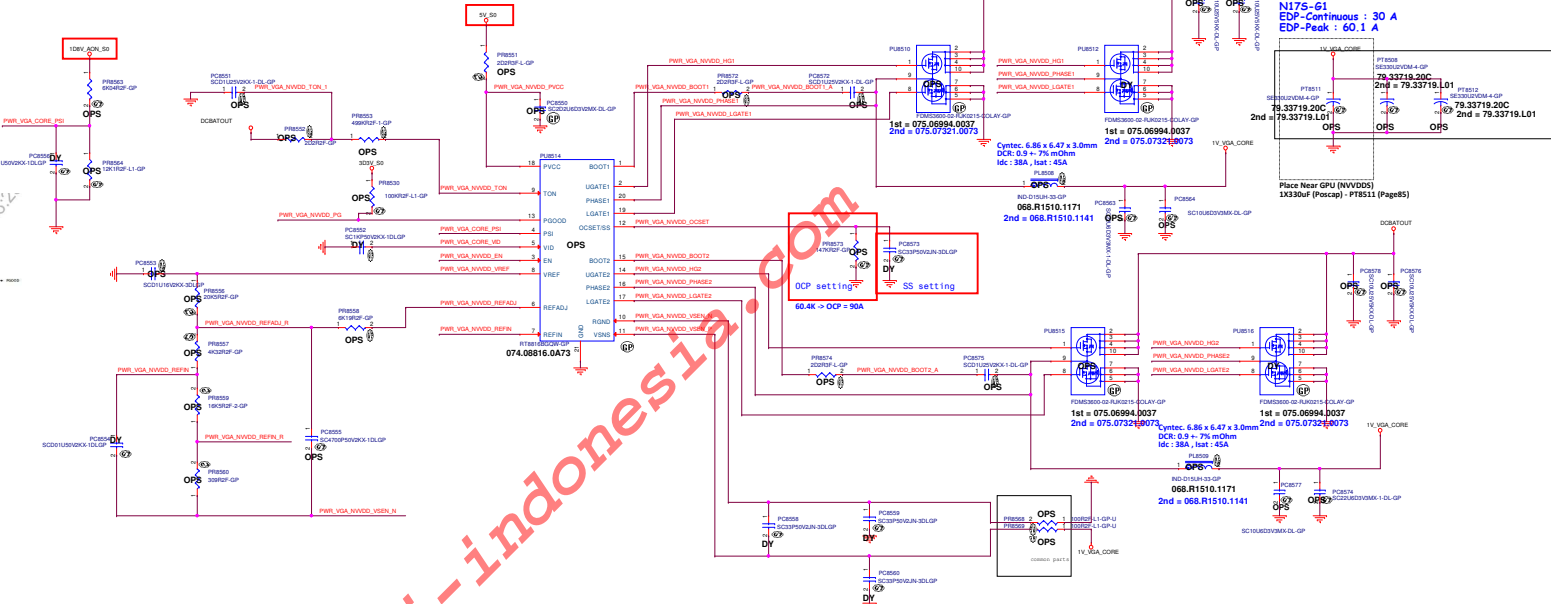
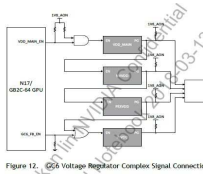
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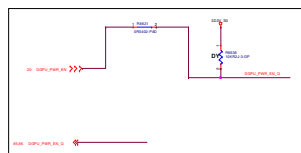
# RT8816B For NVVDD

VGA : N175-G2 / NVVDD  
EDP-Continuous : 28.6A  
EDP-Peak : 60.3A

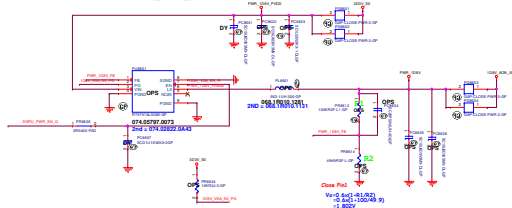


Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

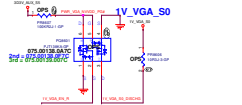




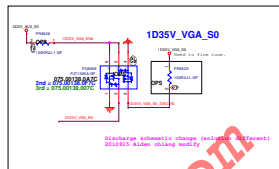
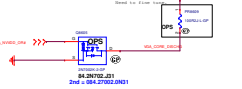
RT5707 for 1.8V\_AON\_S0



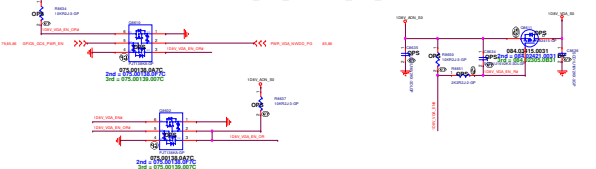
dGPU Power Discharge Circuit



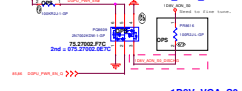
VGA\_CORE



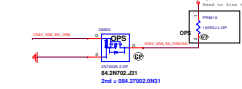
1D8V\_AON\_S0 to 1D8V\_VGA\_S0



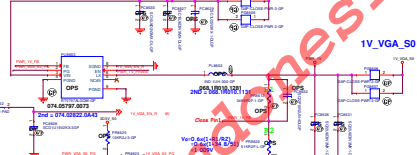
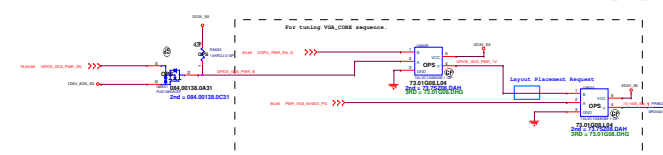
1D8V\_AON\_S0



1D8V\_VGA\_S0

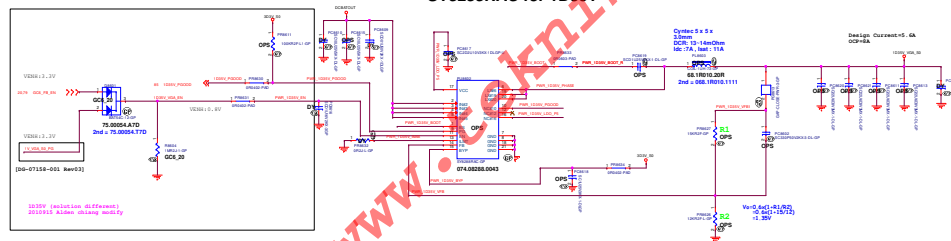


RT5797 for 1V\_VGA\_S0



1D35V\_VGA\_S0

SY8288RAC for 1D35V



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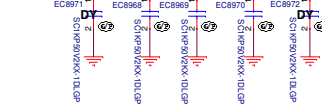
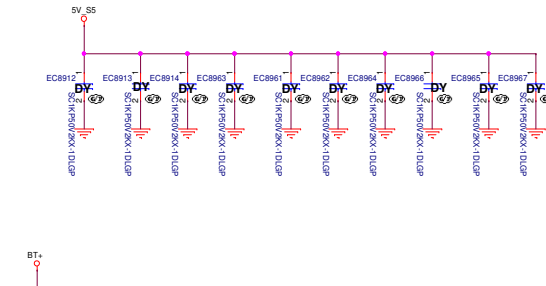
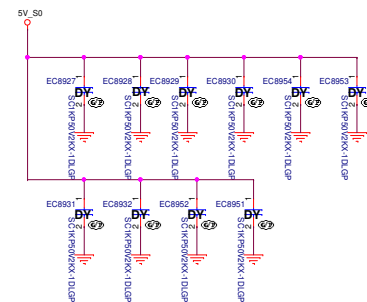
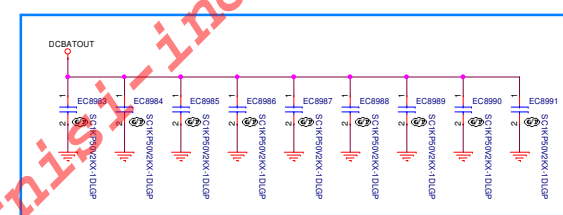
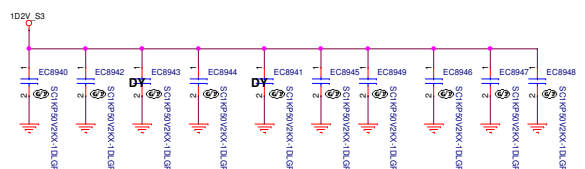
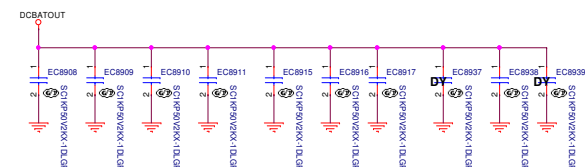
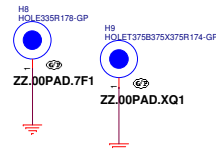
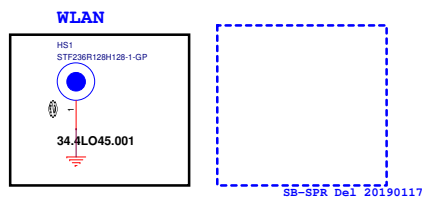
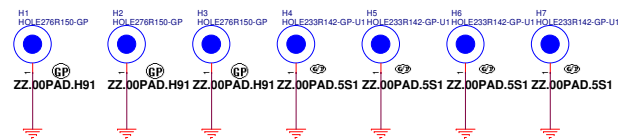
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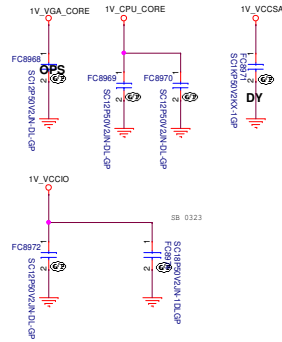
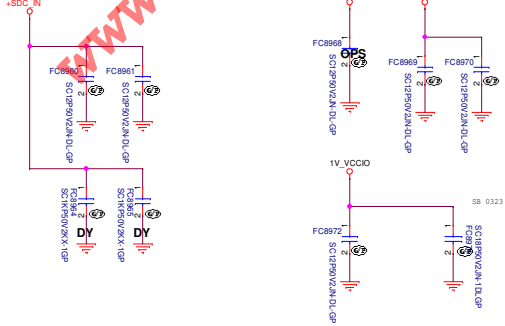
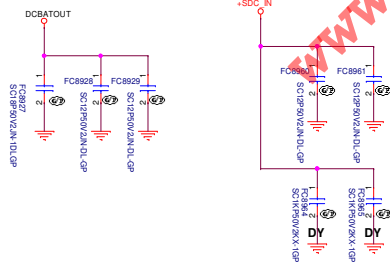
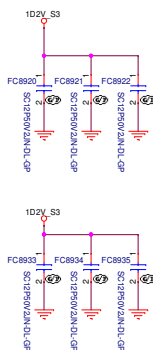
# Main Func = UnusedParts



## SSID = EMI

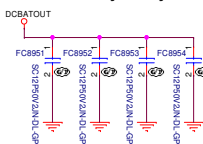
Mind the voltage rating of the caps.

## SSID = RF



## For GPU

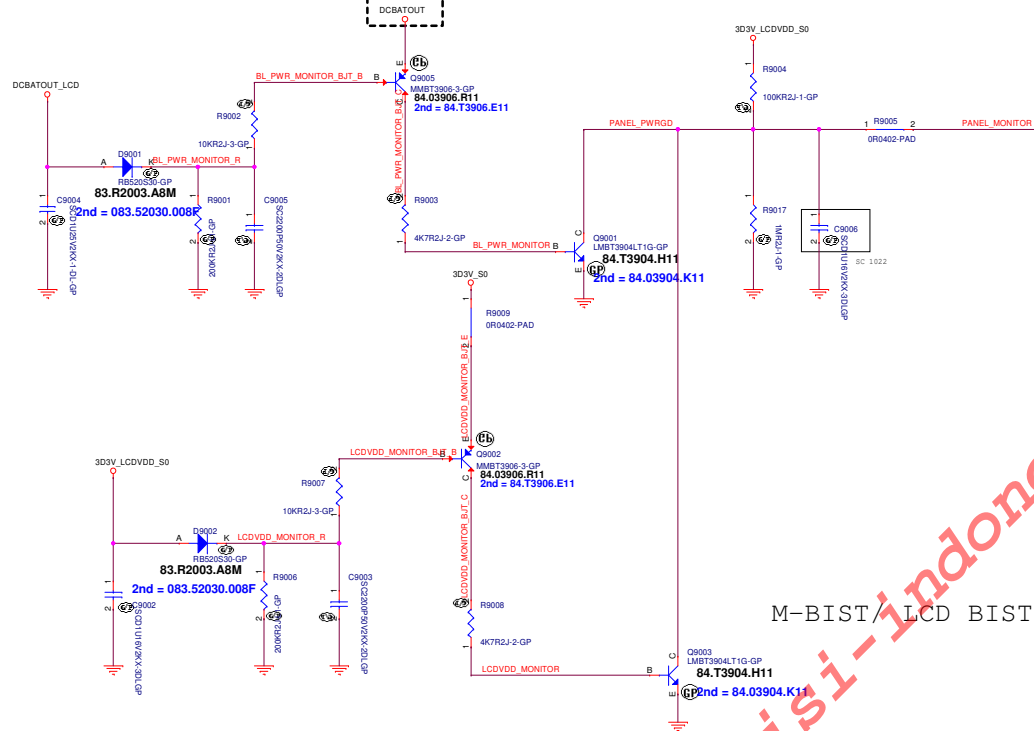
Mind the voltage rating of the caps.



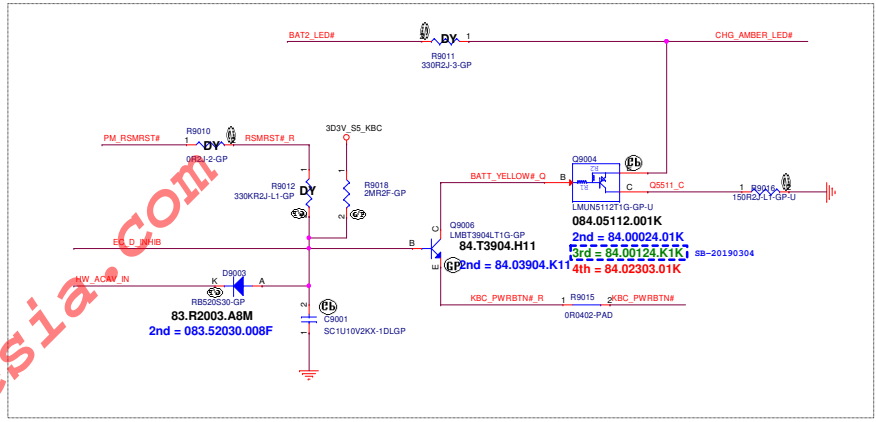
Main FUNC = M-BIST

24.64.90 CHG\_AMBER\_LED# >>>  
24 BAT2\_LED# >>>  
24.66 KBC\_PWRBTN# <<<  
17 PM\_RSMRST# <<<  
24.44 HW\_ACAV\_IN <<<  
24 PANEL\_MONITOR <<<  
24 EC\_D\_INHIB <<<  
24.64.90 CHG\_AMBER\_LED# <<<

LCD BIST for G10 (Was test only for G9)



M-BIST for G10 (Proposed schematic )

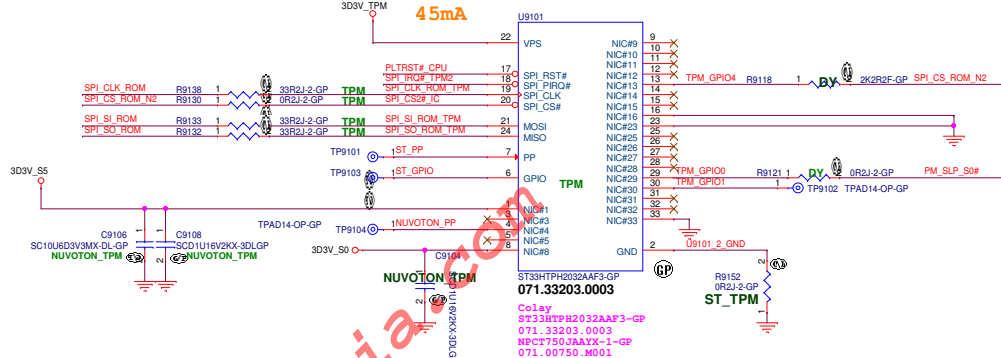
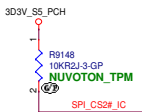
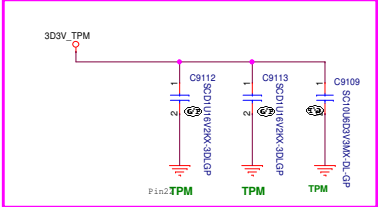


M-BIST/LCD BIST -1890201

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Main Func = TPM

- 18,25 SPI\_SO\_ROM <<< \_\_\_\_\_
- 18,25 SPI\_CLK\_ROM >>> \_\_\_\_\_
- 15,18,25 SPI\_SI\_ROM >>> \_\_\_\_\_
- 18 SPI\_CS\_ROM\_N2 <<< \_\_\_\_\_
- 17,26,61,63,66,71,76 PLTRST#\_CPU >>> \_\_\_\_\_
- 17,24,40 PM\_SLP\_S0# >>> \_\_\_\_\_
- 20 PIRQ# <<< \_\_\_\_\_
- 18 TPM\_SPI\_IRQ# <<< \_\_\_\_\_



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt_L (non TPM)	DY	DY

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***LVDS Switch***

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CRT Switch

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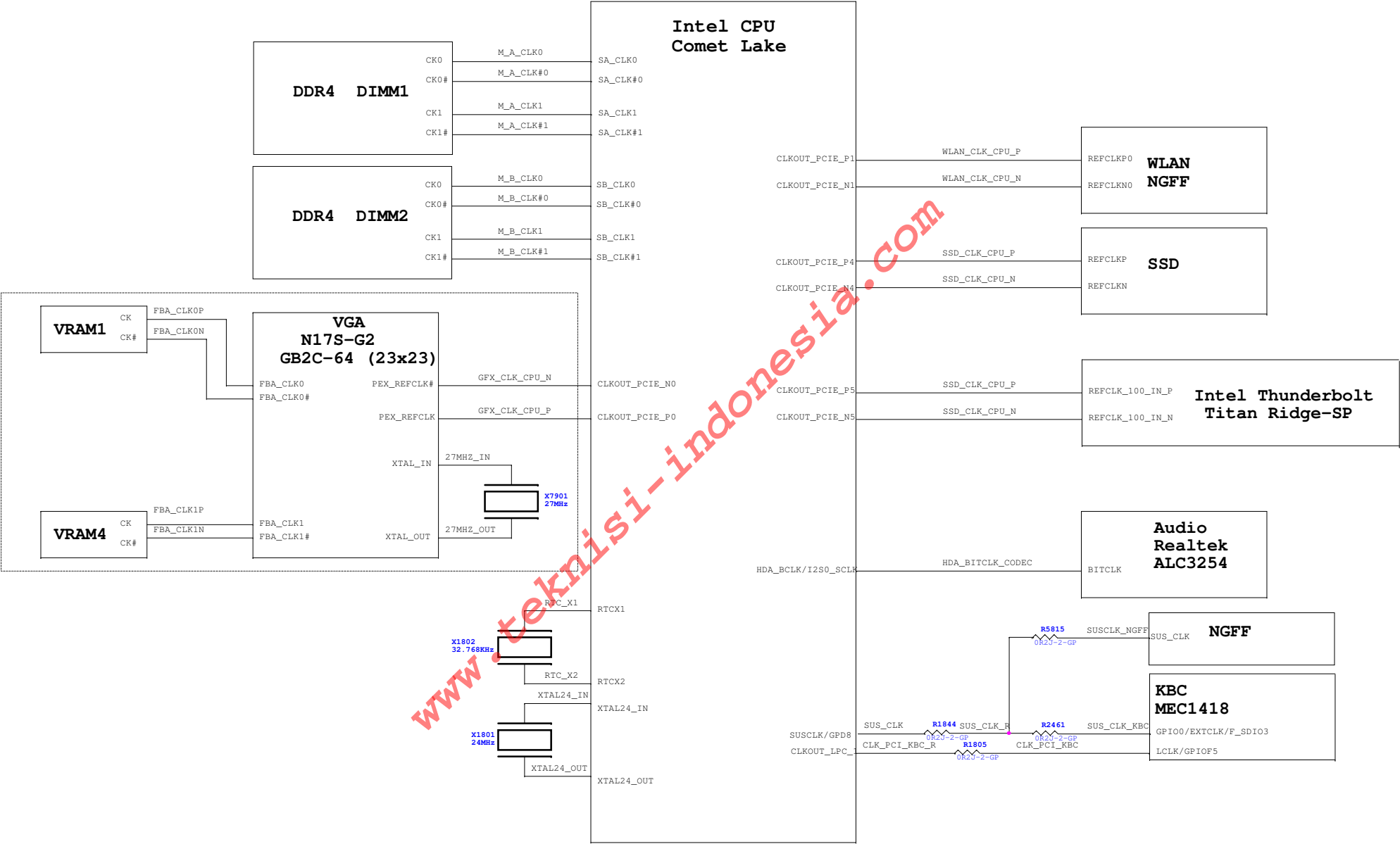
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Main Func = Debug (MIPI)

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CLK Block Diagram



[illegible]

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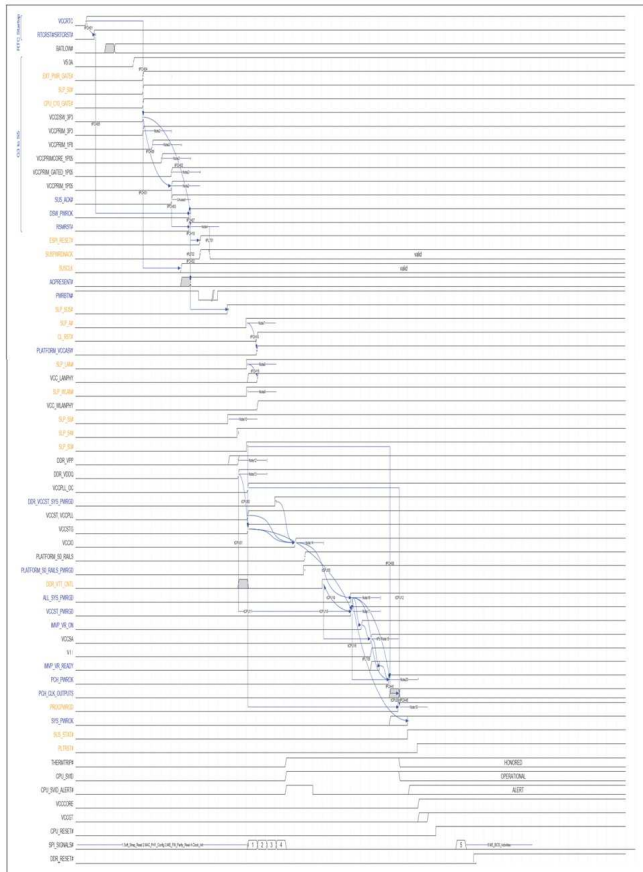
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### CML-U Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



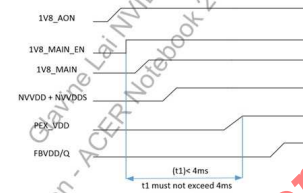
### [dGPU] N17S-G2 Power-Up/Down Sequence

### Power-Up Sequence

The following power-up sequence is required:

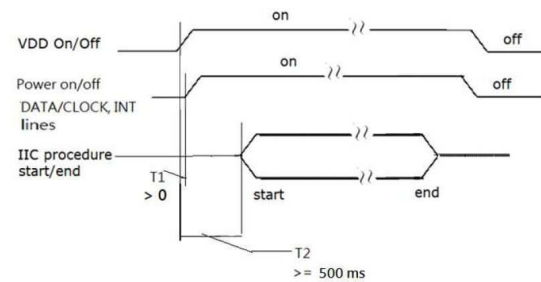
- ▶ 1V8\_AON → 1V8\_MAIN → (NVVDD+ NVVDDS) → PEX\_VDD → FBVDD/Q
- ▶ All GPU power rails must ramp up after 1V8\_AON.
- ▶ FBVDD/Q should ramp up after (NVVDD +NVVDDS) and PEX\_VDD.

All other 1.8V power rails can ramp up with 1V8\_MAIN including PEX\_VDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX\_VDD.

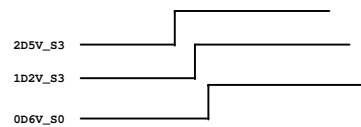


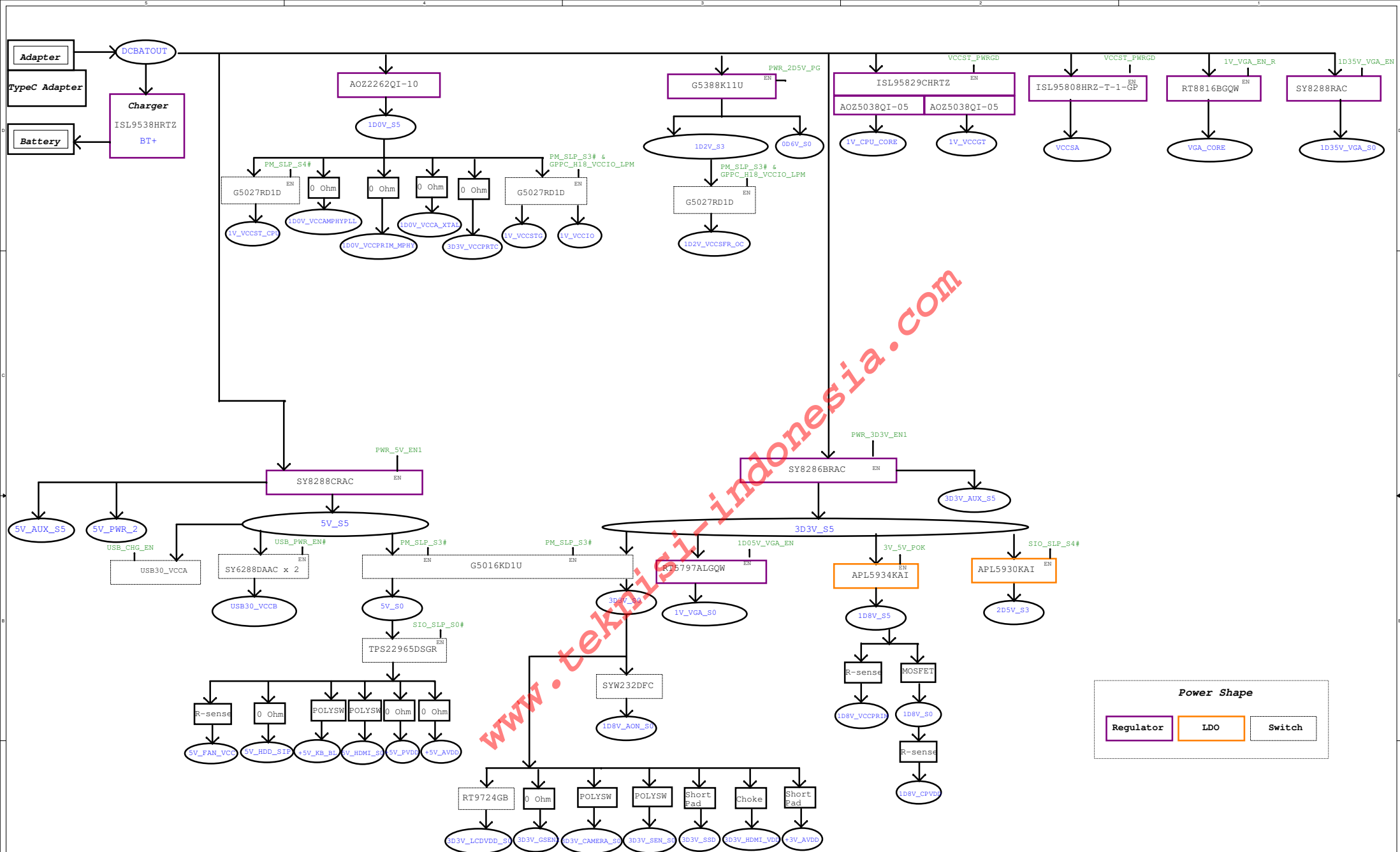
## [TP] Power-Up Sequence

Power on sequency (IIC interface):



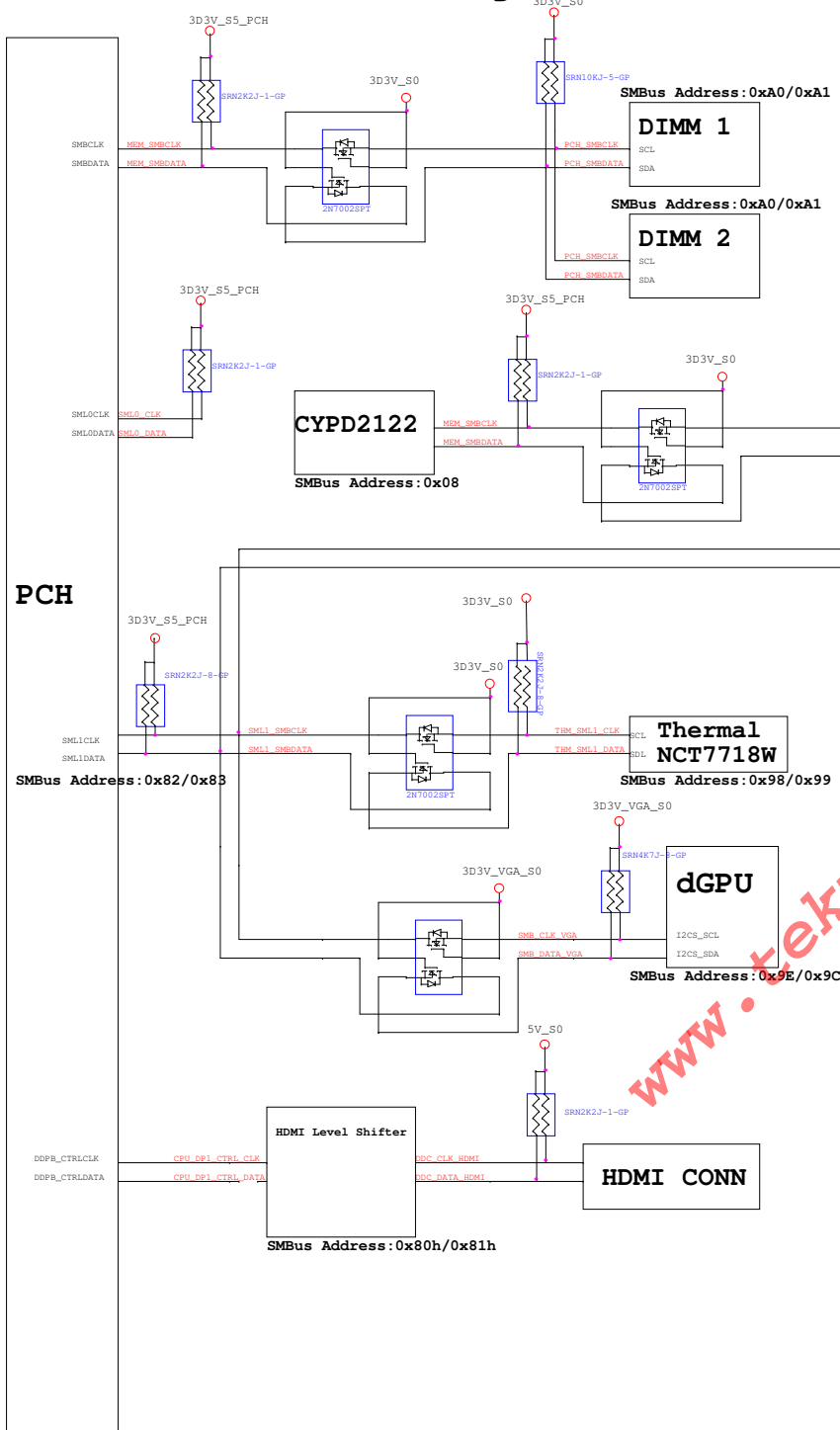
For DDR4 power sequence



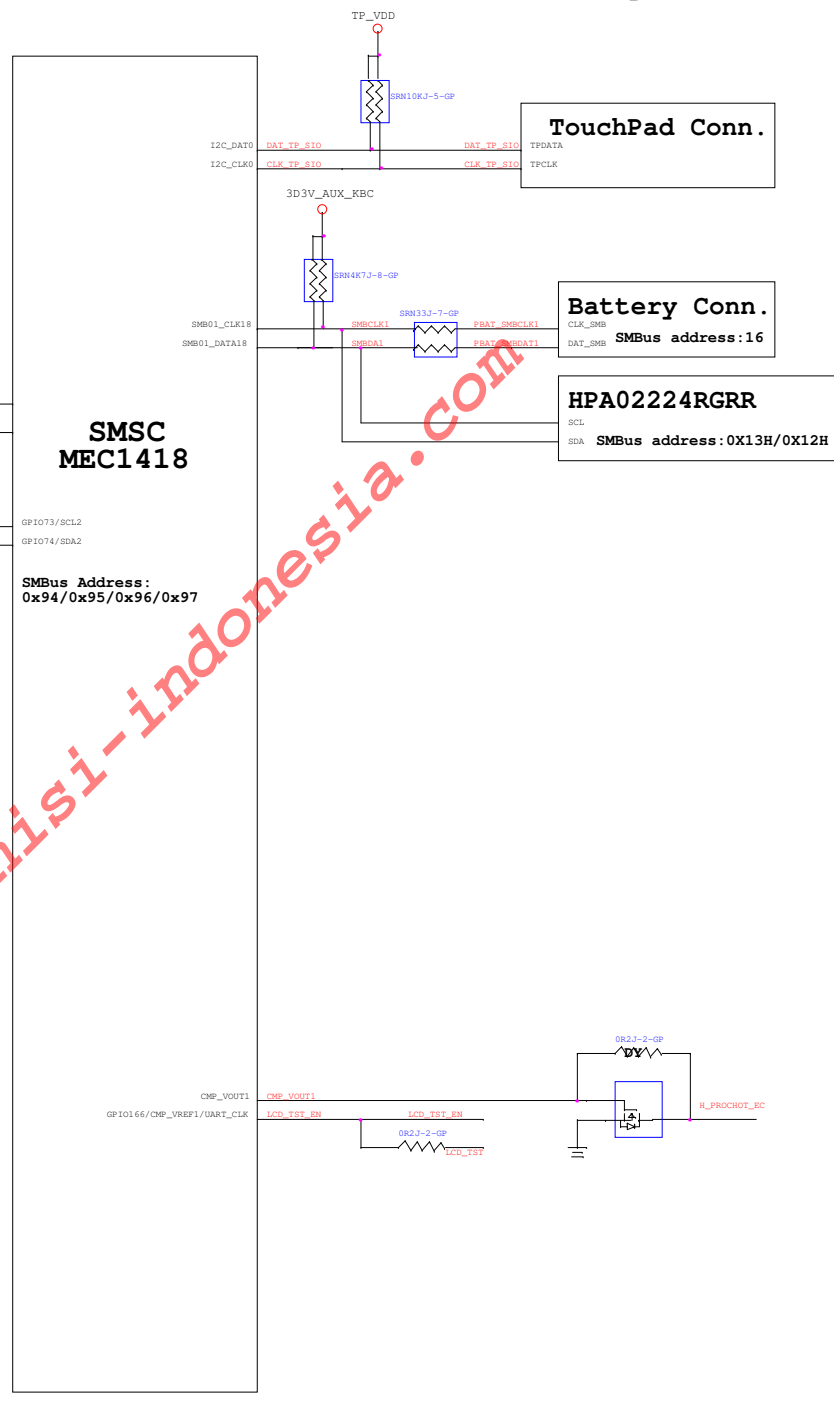


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# PCH SMBus Block Diagram

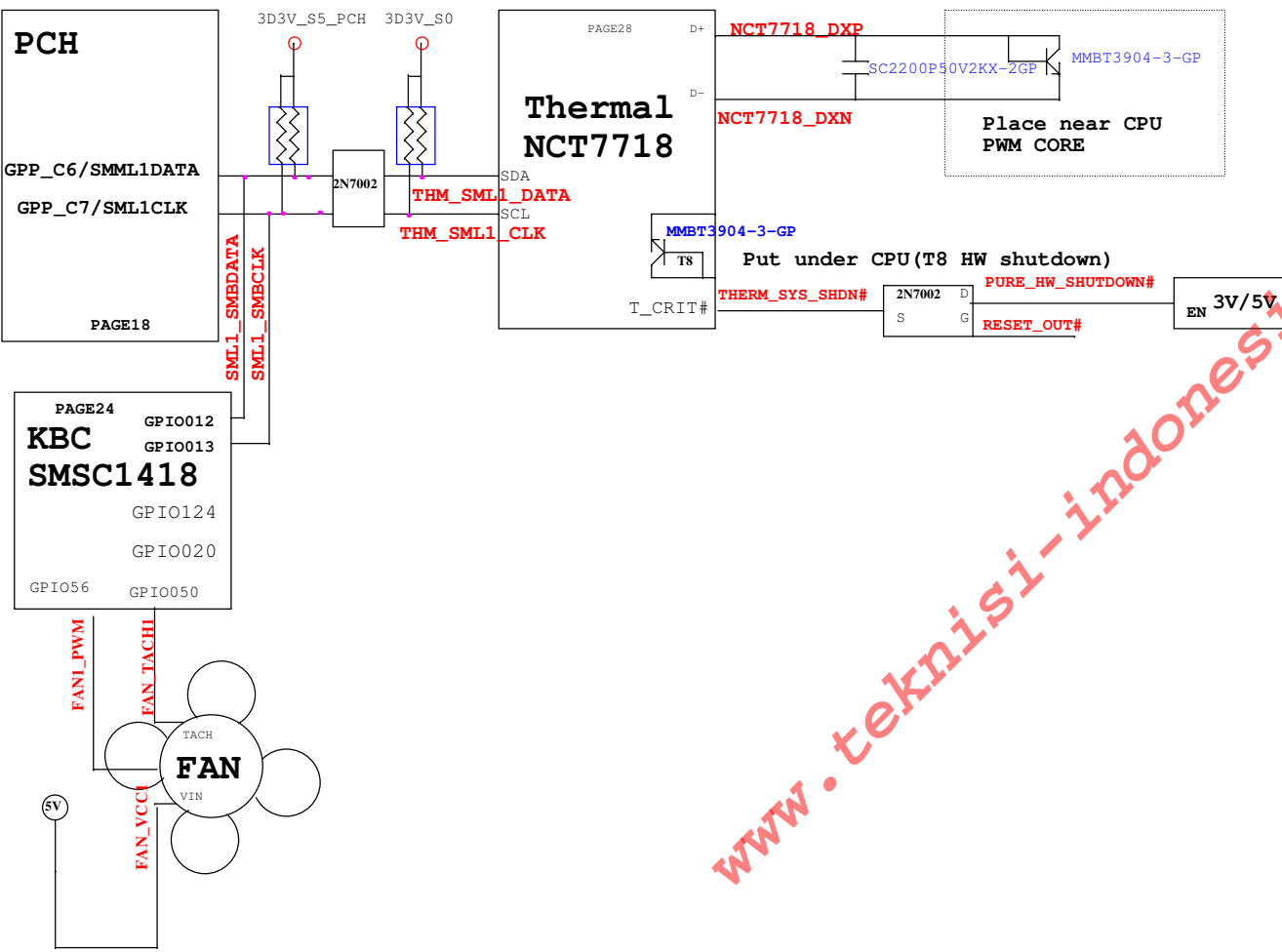


# KBC SMBus Block Diagram

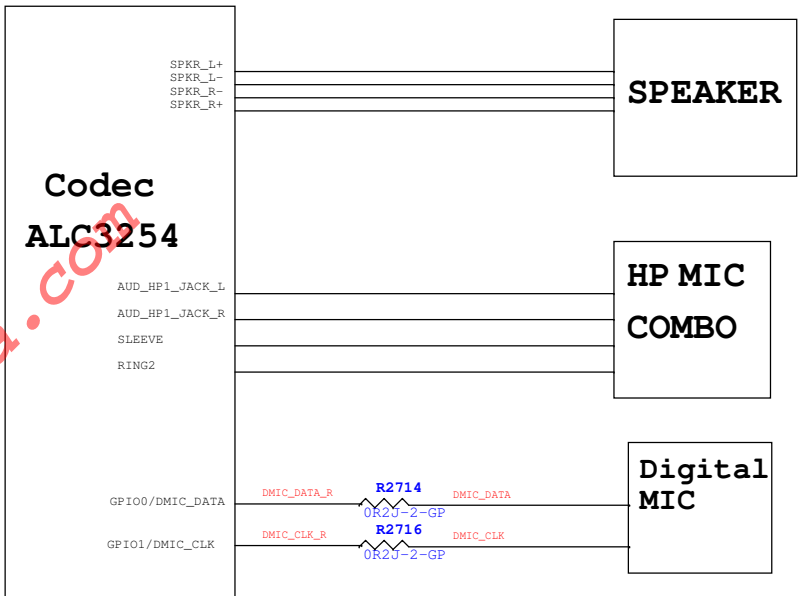




# Thermal Block Diagram



# Audio Block Diagram



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Jedi15"/17" CML



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Title

***SIP connector***

Size  
A

Document Number

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Rev

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